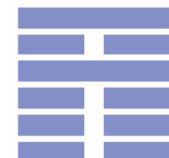


Test and Verification

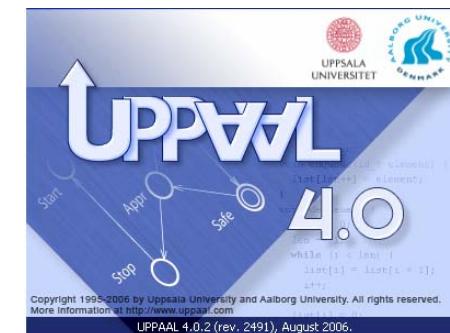
*Of Real-Time Systems
using UPPAAL*

Brian Nielsen

bnielsen@cs.aau.dk



BRICS
Basic Research
in Computer Science



CSS
CENTER FOR INDELREDE SOFTWARE SYSTEMER

Verifikation og Test

Model

```
/* Wait for
void OS_Wait(void);

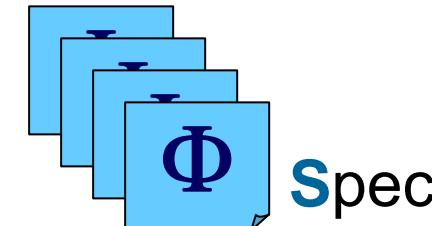
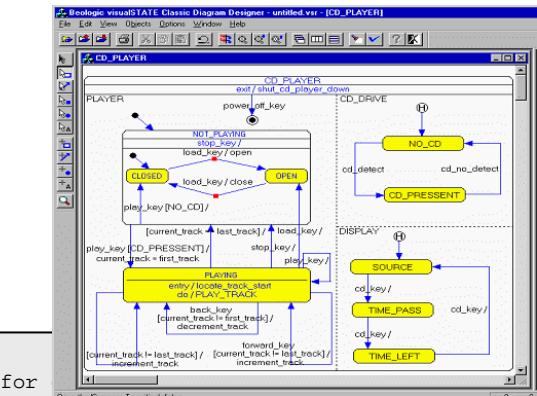
/* Operating system visualSTATE process. Mimics a OS process for a
 * visualSTATE system. In this implementation this is the mainloop
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void OS_VS_Process(void);

/* Define completion code variable. */
unsigned char cc;

void HandleError(unsigned char ccArg)
{
    printf("Error code %c detected, exiting application.\n", ccArg);
    exit(ccArg);
}

/* In d-241 we only use the OS_Wait call. It is used to simulate a
 * system. Its purpose is to generate events. How this is done is up to
 * you.
 */
void OS_Wait(void)
{
    /* Ignore the parameters; just retrieve events from the keyboard and
     * put them into the queue. When EVENT_UNDEFINED is read from the
     * keyboard, return to the calling process. */
    SEM_EVENT_TYPE event;
    int num;
```

Kode



Spec



System

ciss

Verifikation og Test

Model

```
/* Wait for
void OS_Wait(void);

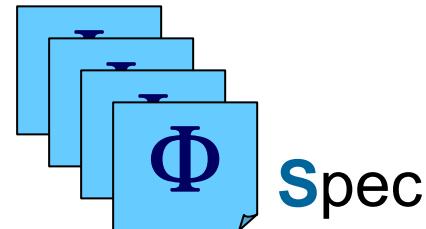
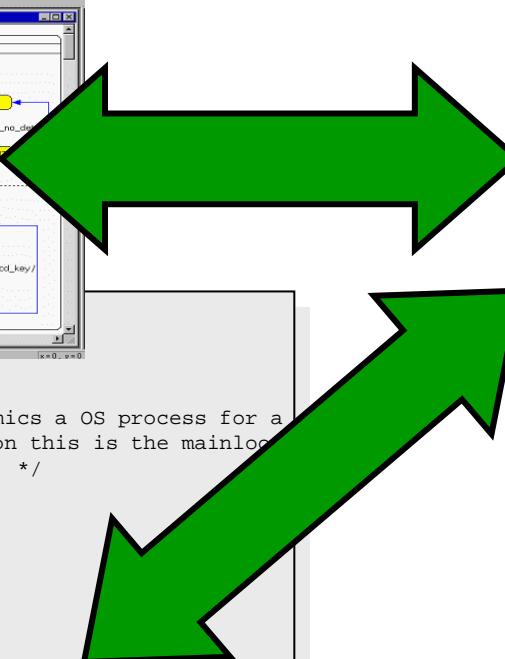
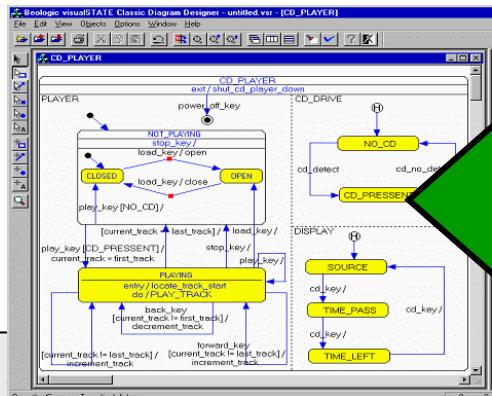
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Kode



Spec



System

ciss

Verifikation og Test

Model

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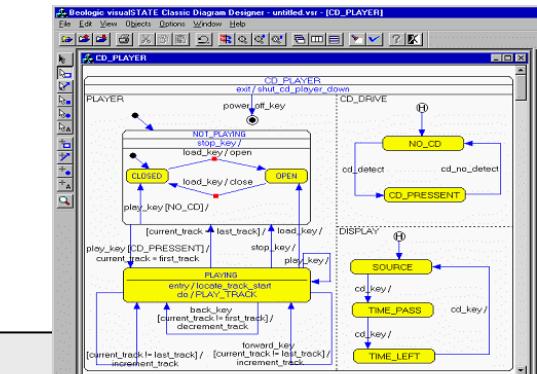
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```

Kode



Spec



System

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Modelling Behaviour using State Machines



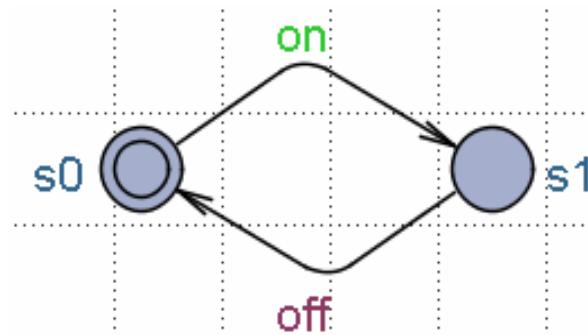
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Modelling processes

- A process is the execution of a sequential program.
- modeled as a finite state machine (LTS)
 - ✿ transits from state to state
 - ✿ by executing a sequence of *atomic* actions.

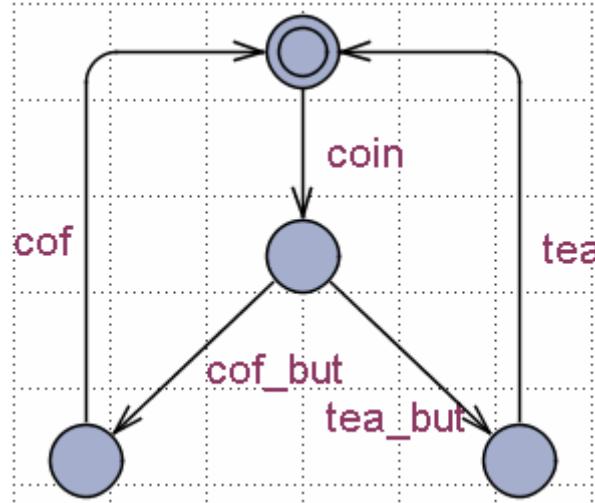
a light switch
LTS



on → off → on → off → on → off →

a sequence of
actions or *trace*

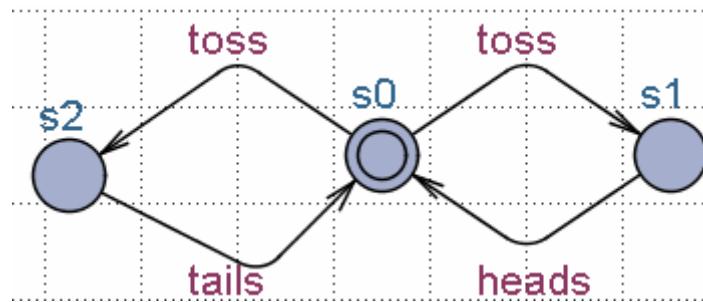
Modelling Choices



- Who or what makes the choice?
- Is there a difference between input and output actions?

Non-deterministic Choice

■ Tossing a coin



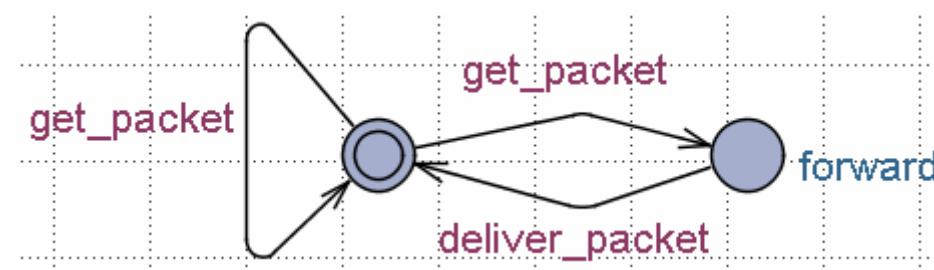
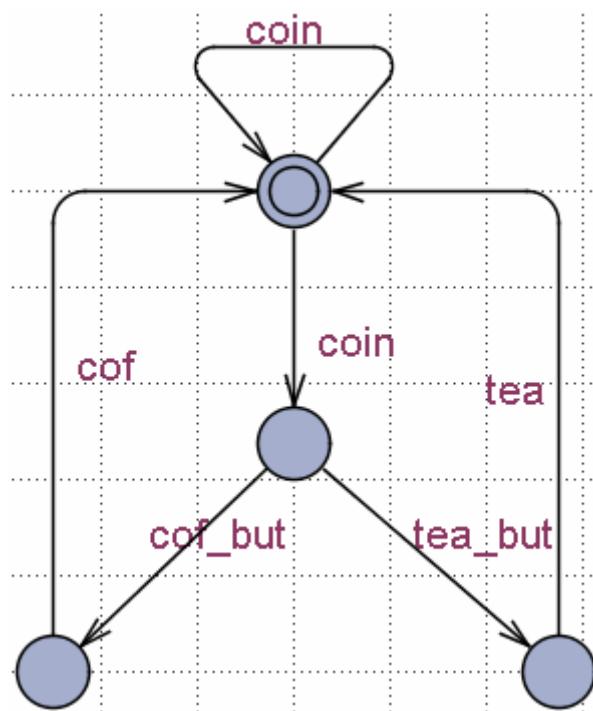
■ Possible traces?

- ✳ Both outcomes possible
- ✳ Nothing said about relative frequency
- ✳ If coin is fair, the outcome is 50/50

Non-Deterministic Choice -modelling failure

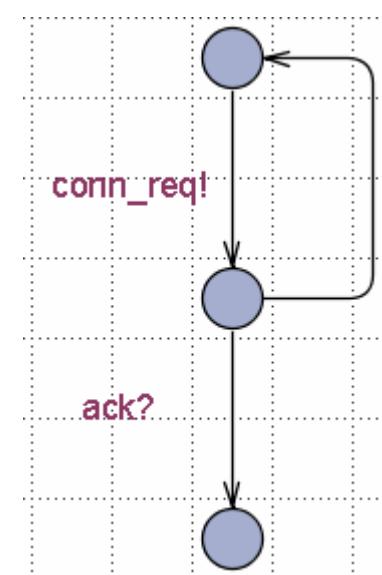
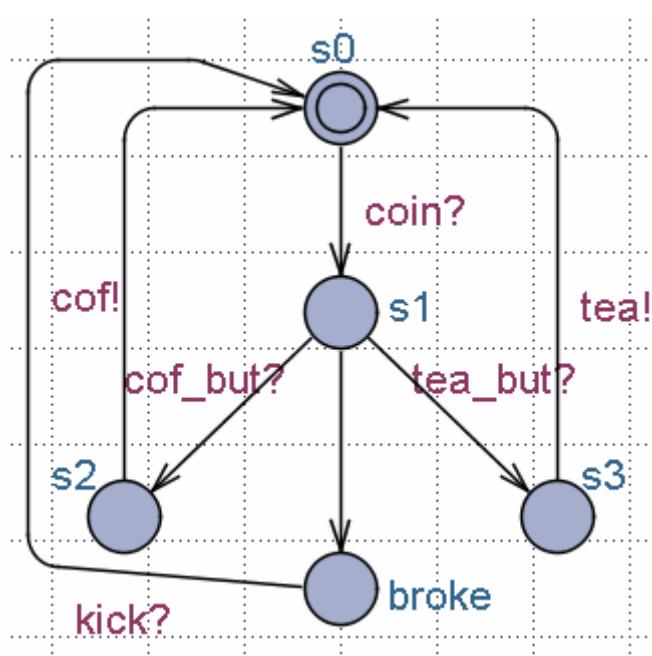
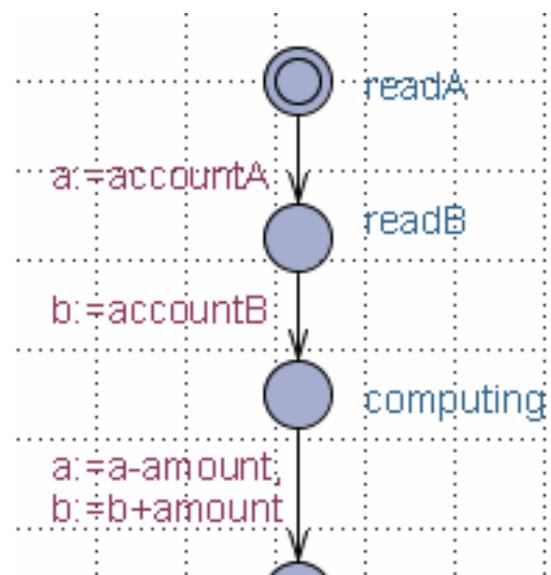
How do we model an unreliable communication channel which accepts **packets**, and if a failure occurs produces no output, otherwise **delivers** the packet to the receiver?

Use non-determinism...



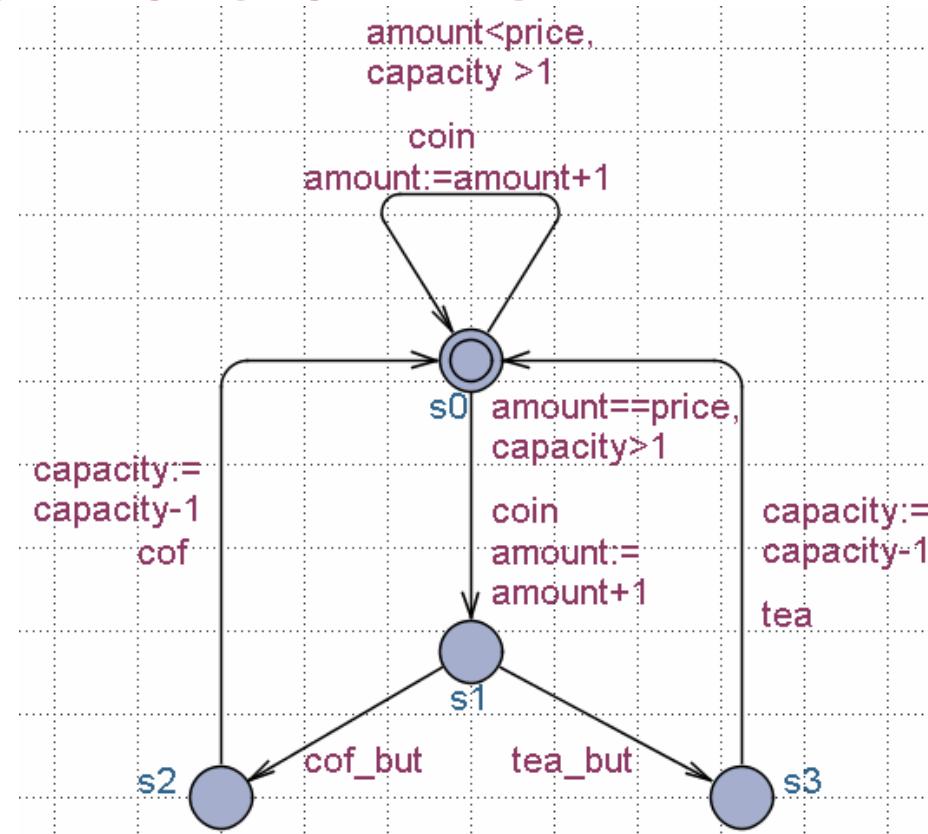
Internal-Actions

- Spontaneous actions
- Internal actions
- Tau-actions
- Internal transitions can be taken on the initiative of a single machine without communication with others



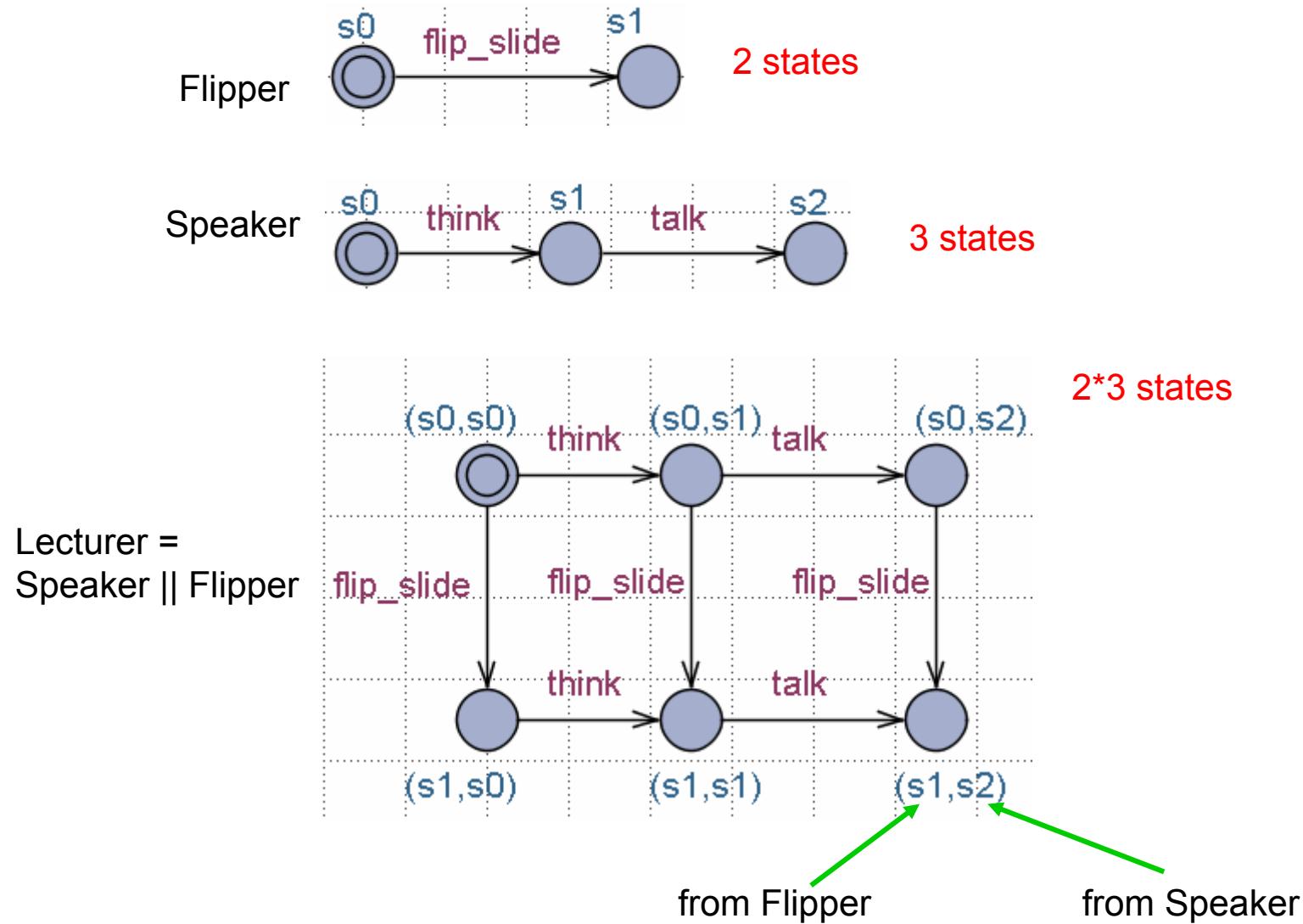
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Extended FSM



- EFSM = FSM + **variables** + **enabling conditions** + **assignments**
- Transition still atomic
- Can be translated into FSM if variables have bounded domain
- State: control location+variable states: (state,total,capacity)
- $(s_0, 5, 10)$

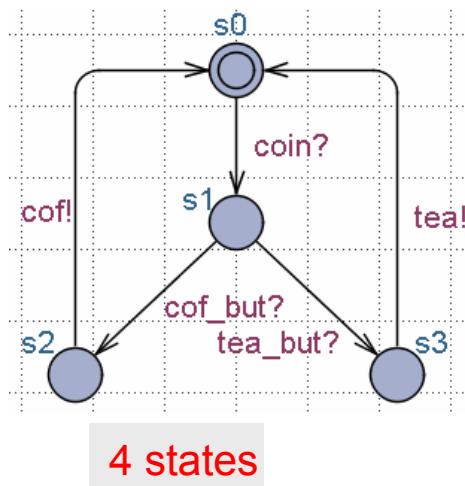
Parallel Composition: interleaving



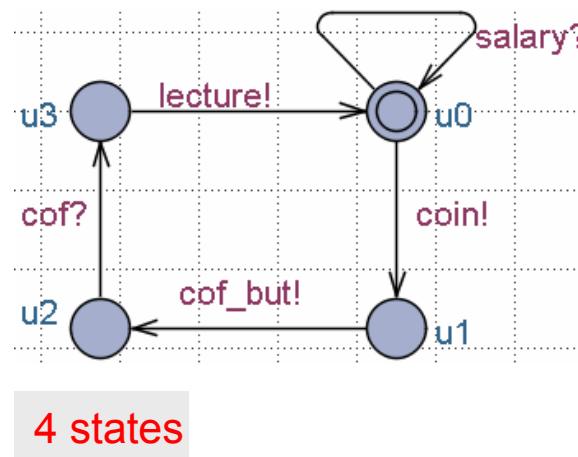
Process Interaction

- ! = Output, ? = Input
- Handshake communication
- Two-way

Coffee Machine



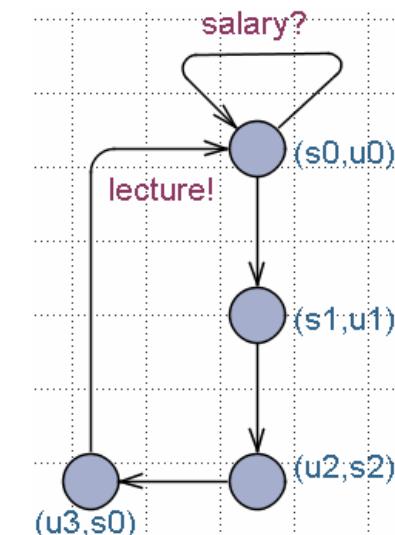
Lecturer



synchronization results in internal actions

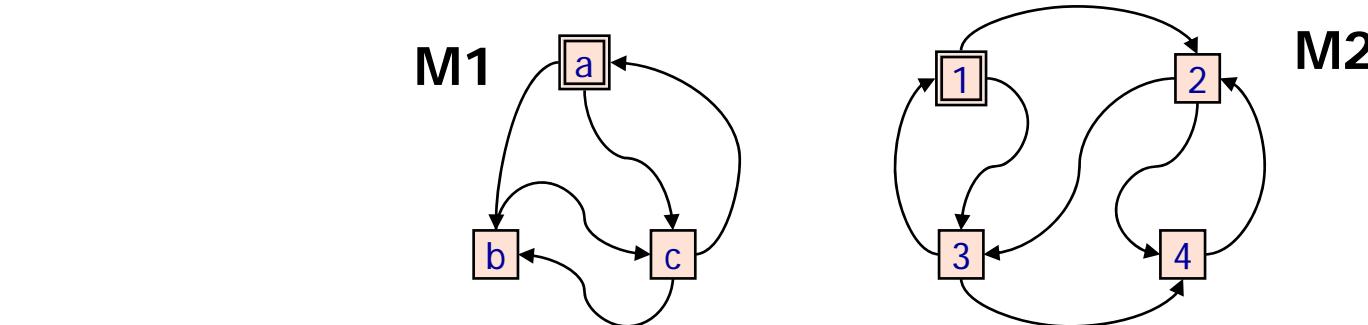
4 states: Interaction constrain overall behavior

University=
Coffee Machine || Lecturer
• LTS?
• How many states?
• Traces ?

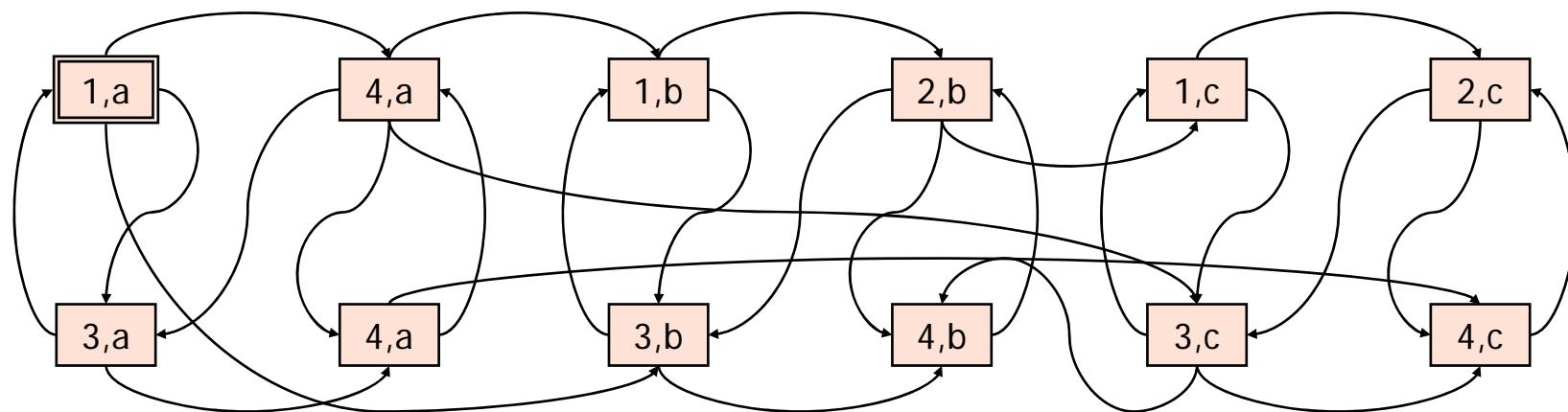


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Composition



M1 x M2



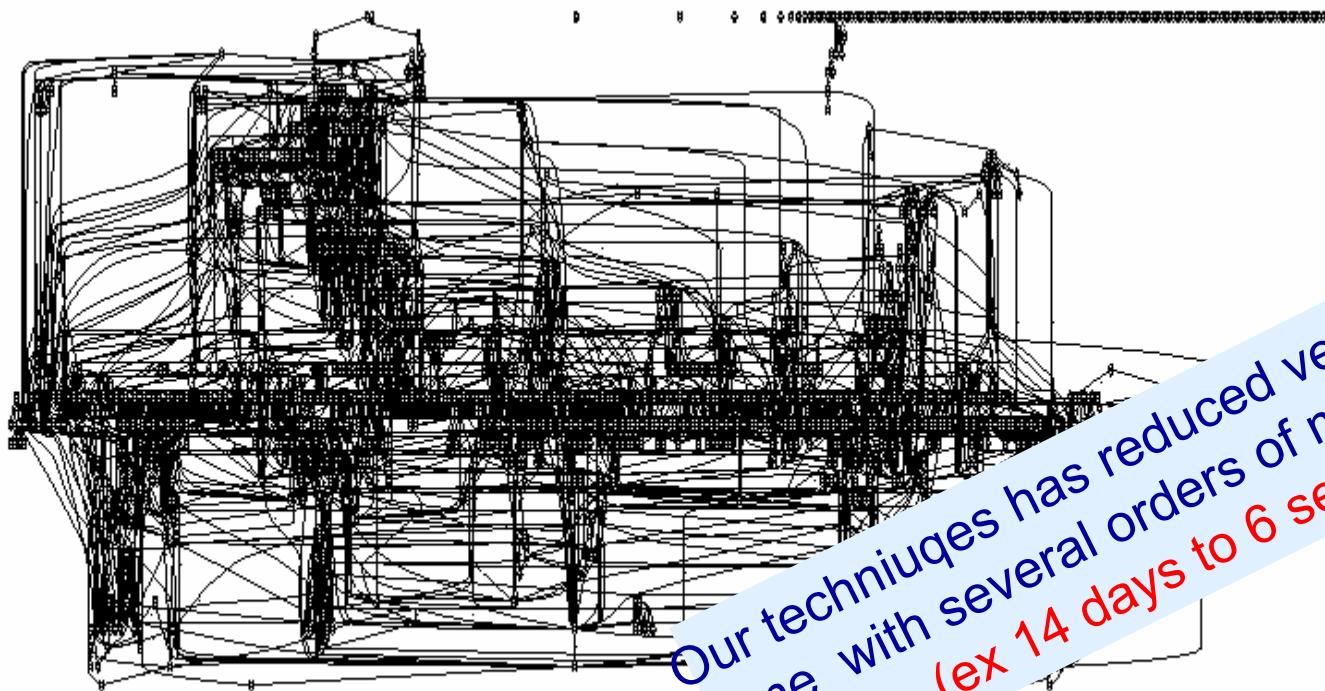
All combinations=
exponential in no of machines

Train Simulator

VVS
visualSTATE

1421 machines
11102 transitions
2981 inputs
2667 outputs
3204 local states
Declare state sp.: 10^{476}

BUGS ?

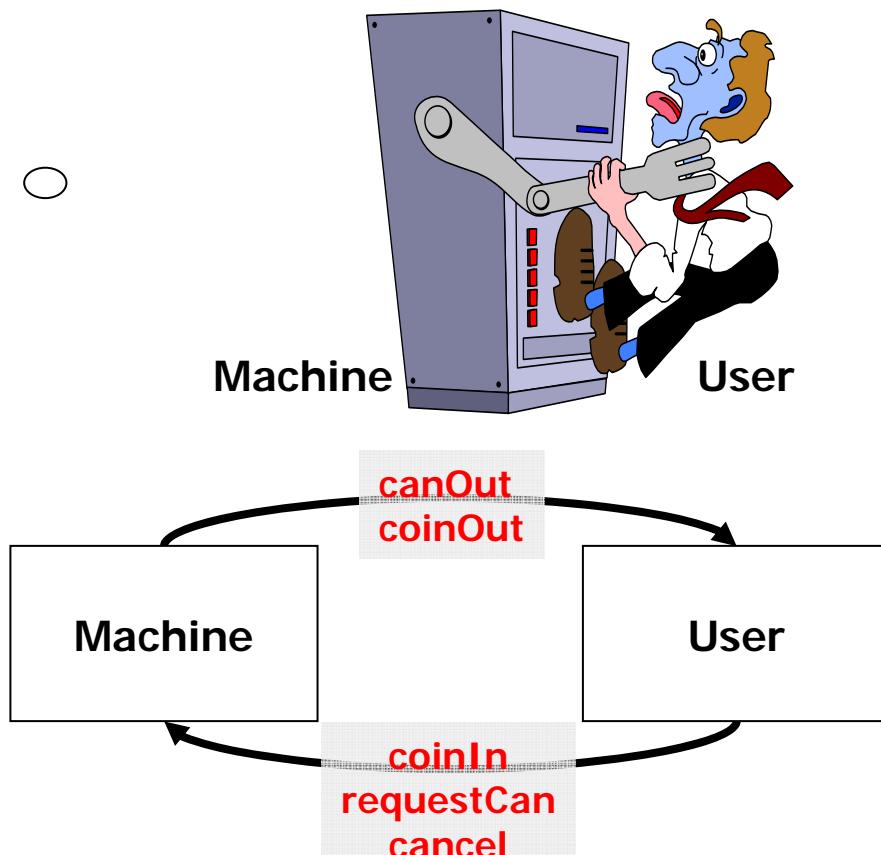


Our techniques has reduced verification
time with several orders of magnitude
(ex 14 days to 6 sec)

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Modelling Exercise

The Vending Machine



- Simulate model w Random User
- Model Fair User
- Model Non-Thirsty User
- Deadlocks ?
- Cans requested will be delivered ?
- Cancellations are obeyed ?
- What happens if multiple users?

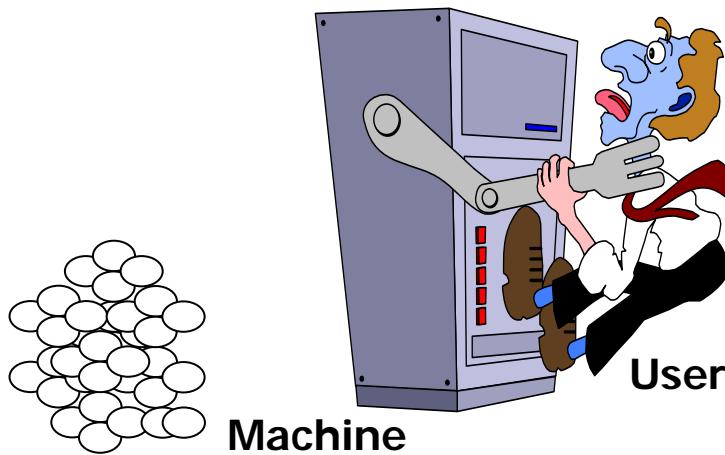
Assumption: 1 can = 1 coin!

Exercise

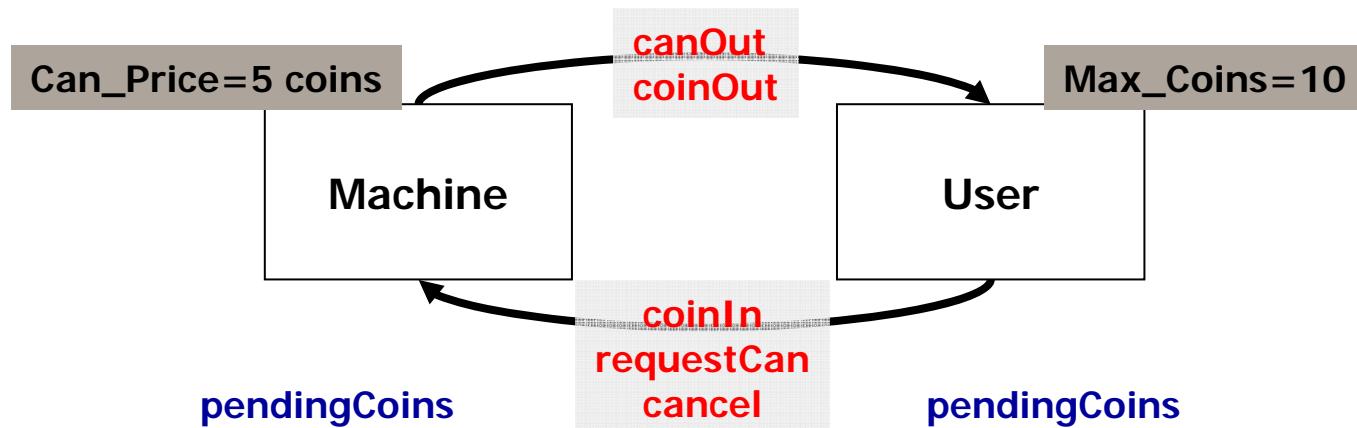
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Modelling Exercise

The Vending Machine



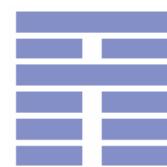
- Extend model of Machine and FairUser
- Do extensive simulation



Exercise
CISS

Verification = Model Checking

- Reachability
- Generic properties

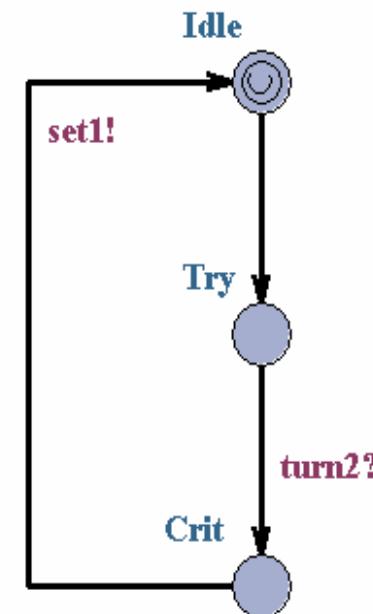
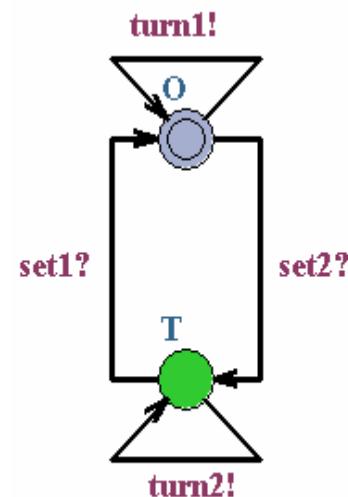
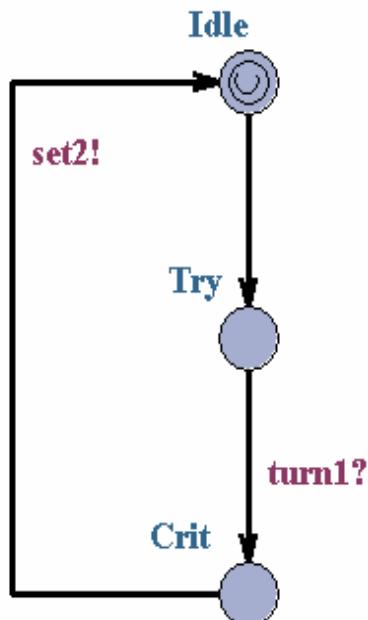


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Basic Research
in Computer Science

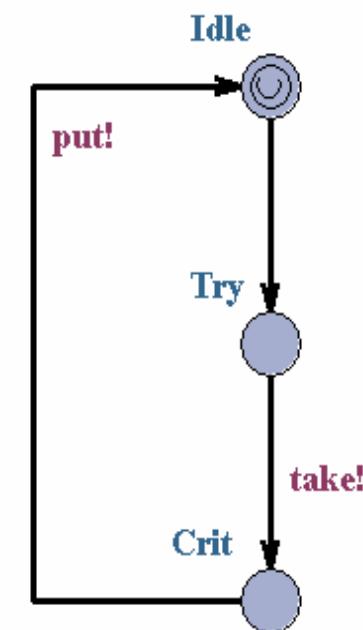
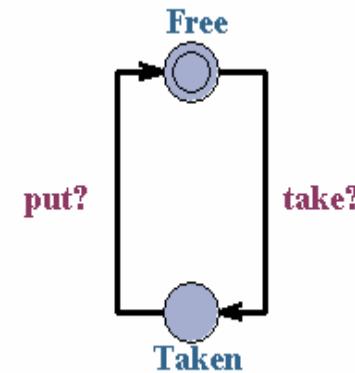
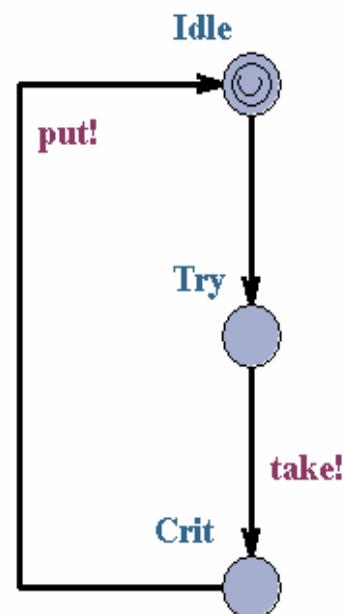
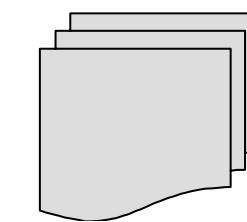
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Mutual Exclusion

Taking turns

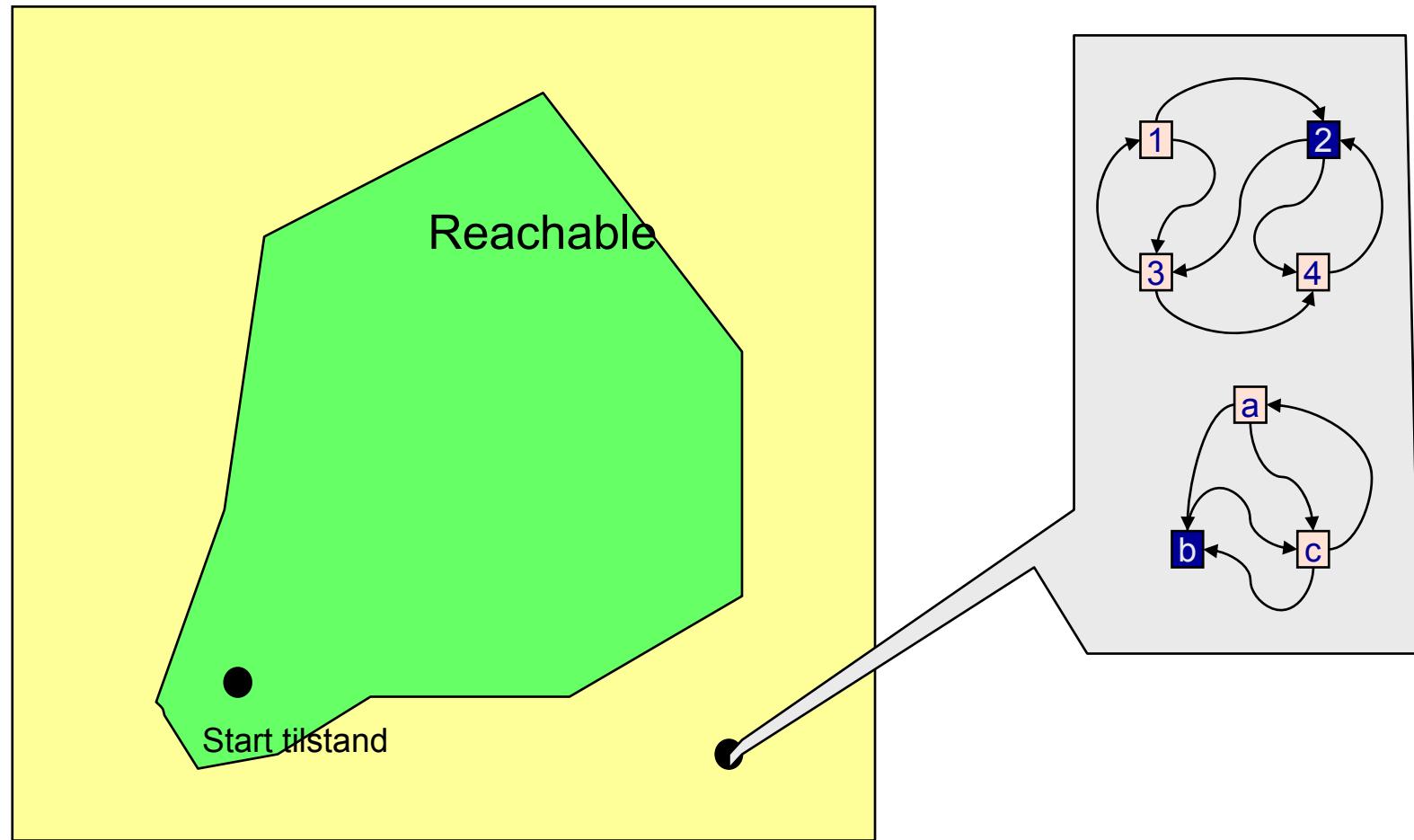


Mutual Exclusion



Udforskning af Tilstandsrum

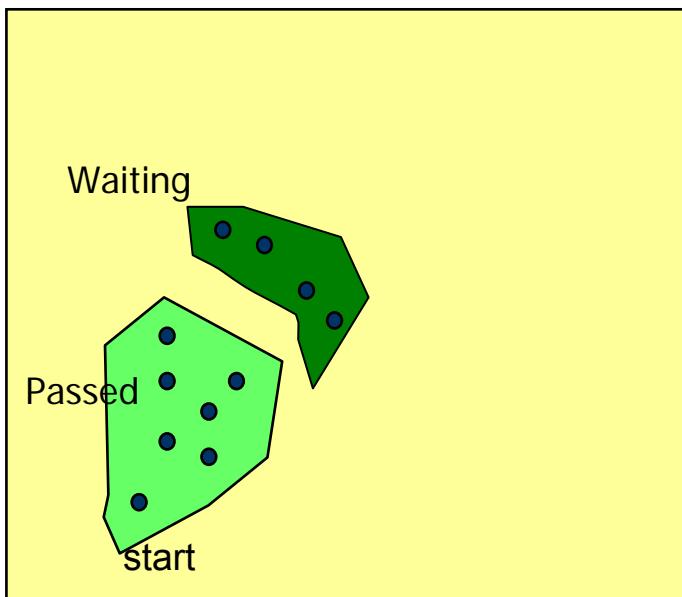
Erklæret tilstandsrum



Udforskning af tilstandrum

Forward Reachability Analysis

Erklæret tilstandsrum

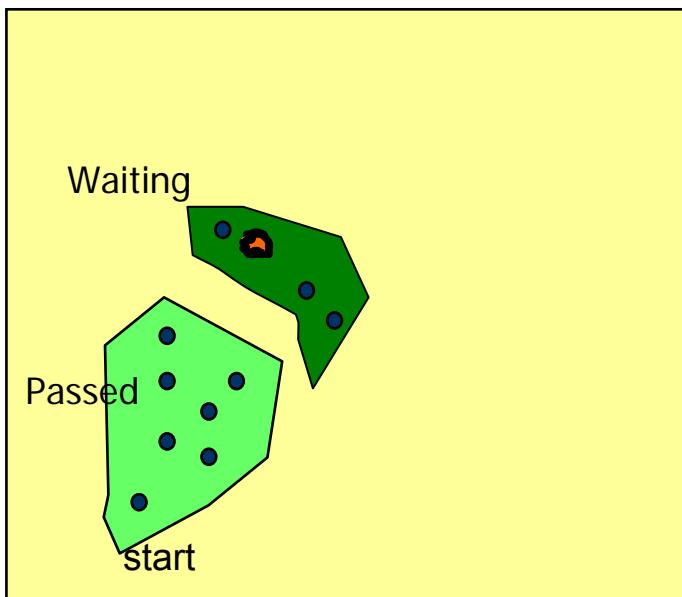


```
Passed := ∅  
Waiting := {s0}  
While (Waiting != ∅)  
{  
    select s ∈ Waiting  
    Waiting := Waiting \ {s}  
    if s ∉ Passed  
        whenever (s → t) then  
            Waiting := Waiting ∪ {t}  
    Passed := Passed ∪ {s}  
}
```

Udforskning af tilstandrum

Forward Reachability Analysis

Erklæret tilstandsrum

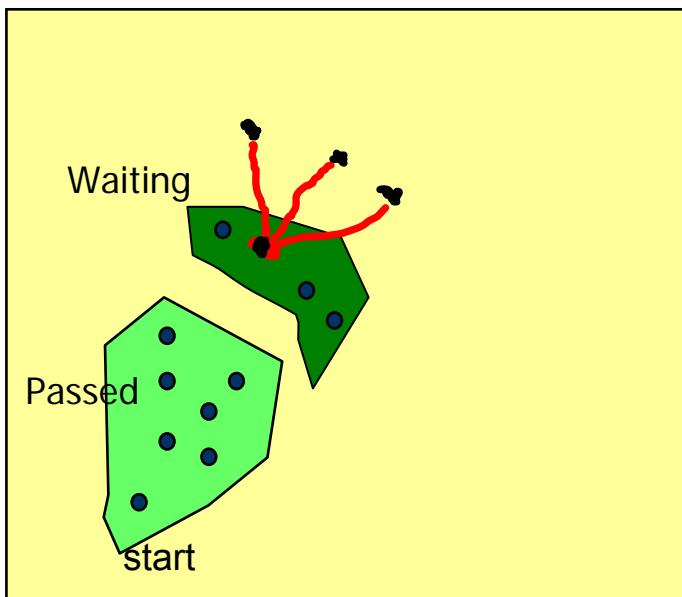


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Udforskning af tilstandrum

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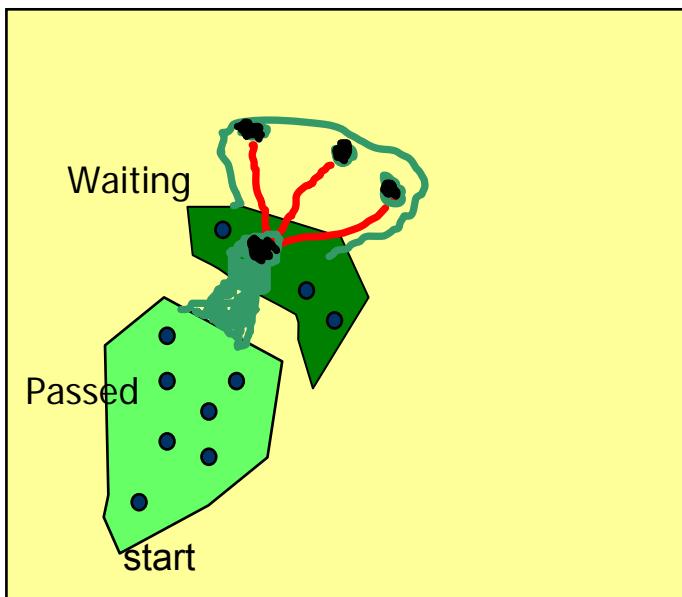


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Udforskning af tilstandrum

Forward Reachability Analysis

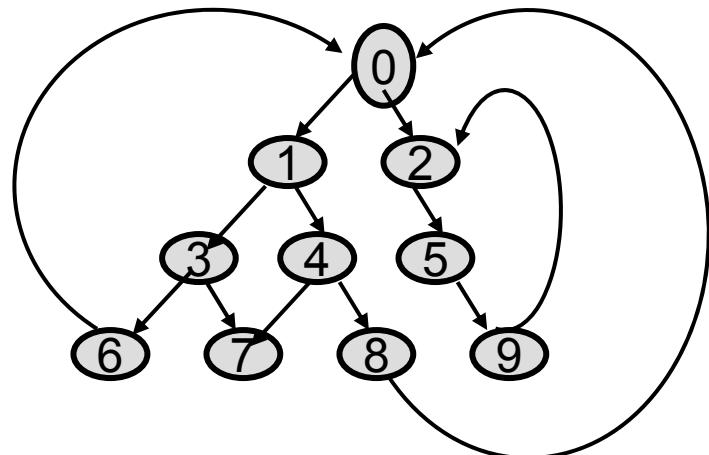
Erklæret tilstandsrum



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While (Waiting != ∅)  
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Udforskning af tilstandrum

Forward Reachability Analysis

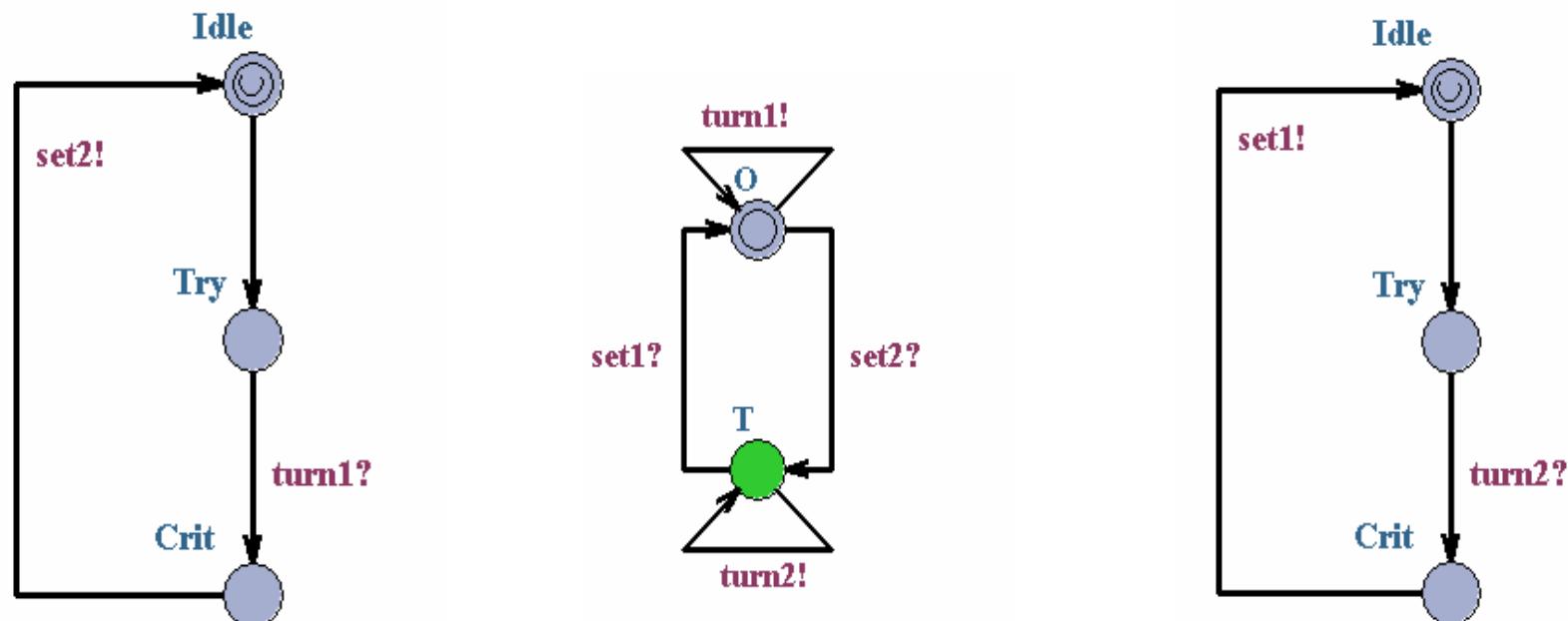


```
Passed :=  $\emptyset$ 
Waiting := { $s_0$ }
while (Waiting !=  $\emptyset$ )
{
    select  $s \in$  Waiting
    Waiting := Waiting \ { $s$ }
    if  $s \notin$  Passed
        whenever ( $s \rightarrow t$ ) then
            Waiting := Waiting  $\cup$  { $t$ }
    Passed := Passed  $\cup$  { $s$ }
}
```

Depth-first search: organize Waiting as a **Stack**
Order: 0 1 3 6 7 4 8 2 5 9

Breadth-first search: organize Waiting as a **Queue**
Order: 0 1 2 3 4 5 6 7 8 9

Gensidig Udelukkelse

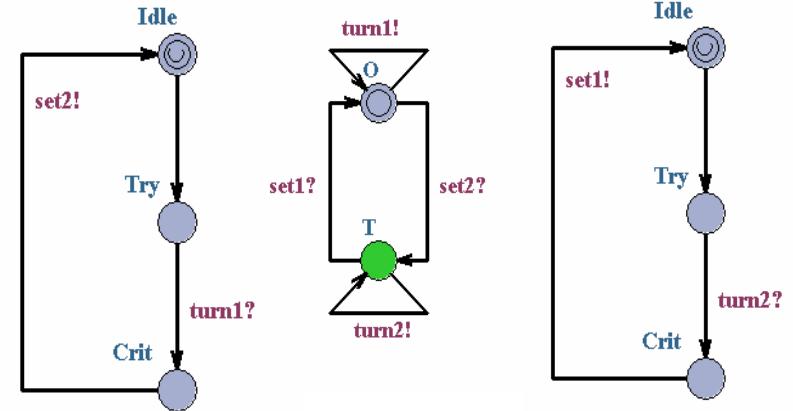
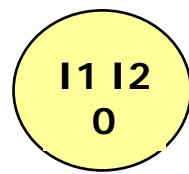


Turn

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Gensidig udelukkelse

Forward Reachability

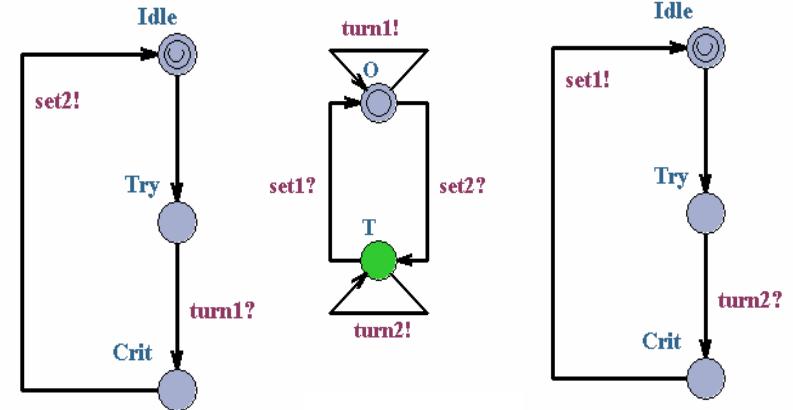
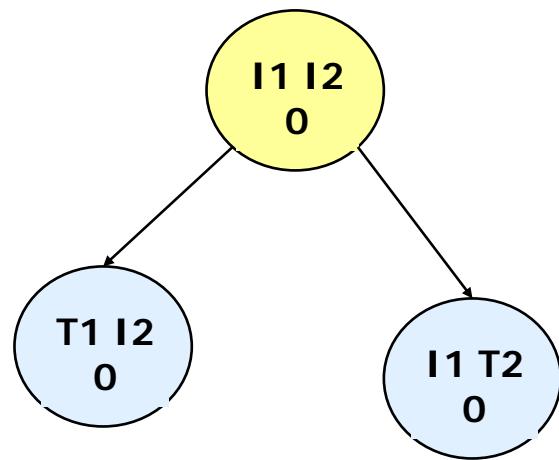


Turn

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Gensidig udelukkelse

Forward Reachability

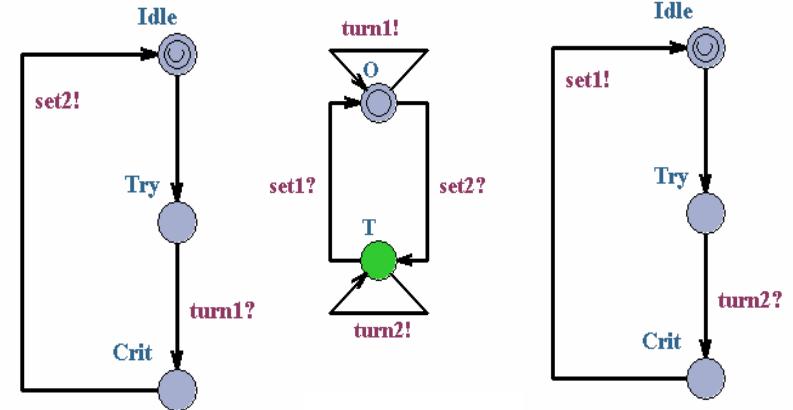
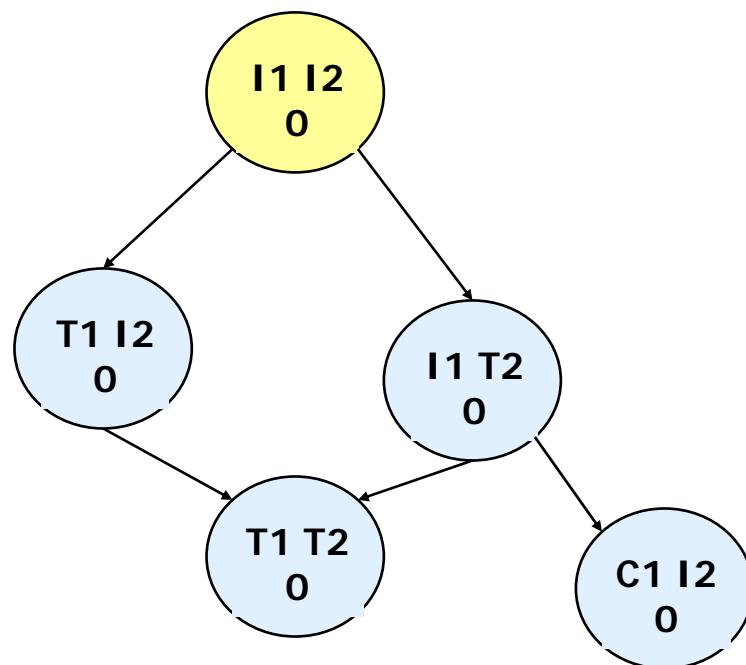


Turn

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Gensidig udelukkelse

Forward Reachability

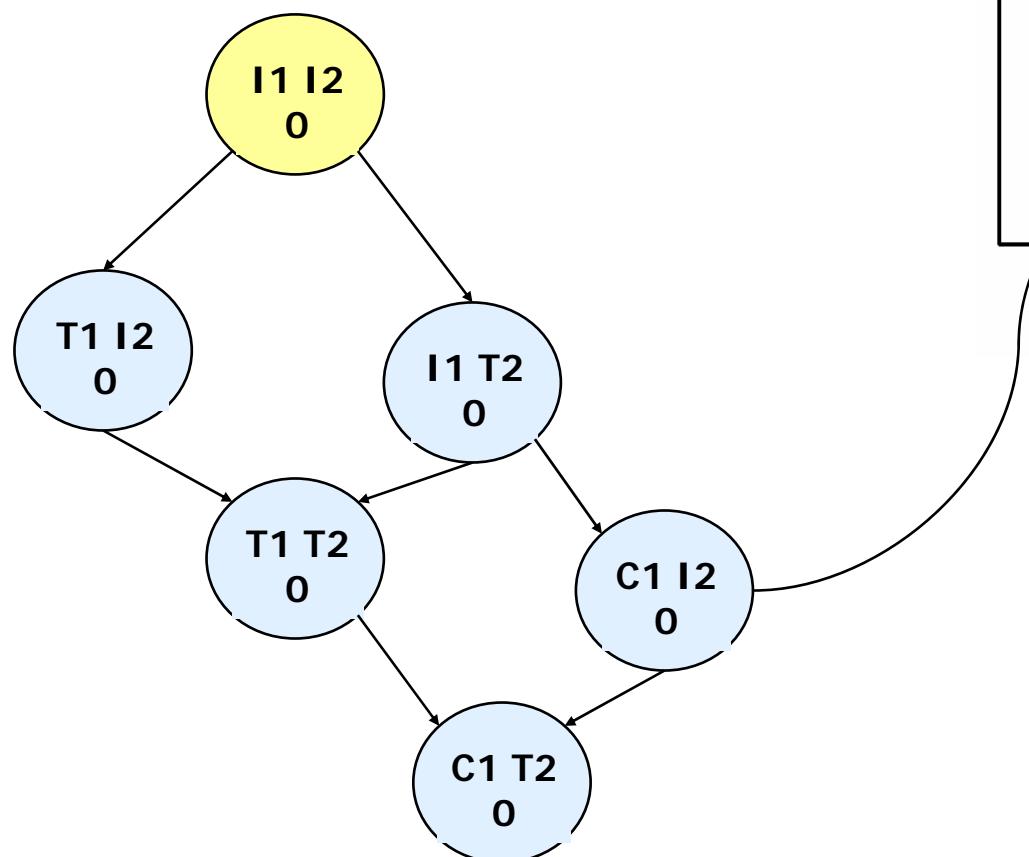


Turn

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Gensidig udelukkelse

Forward Reachability

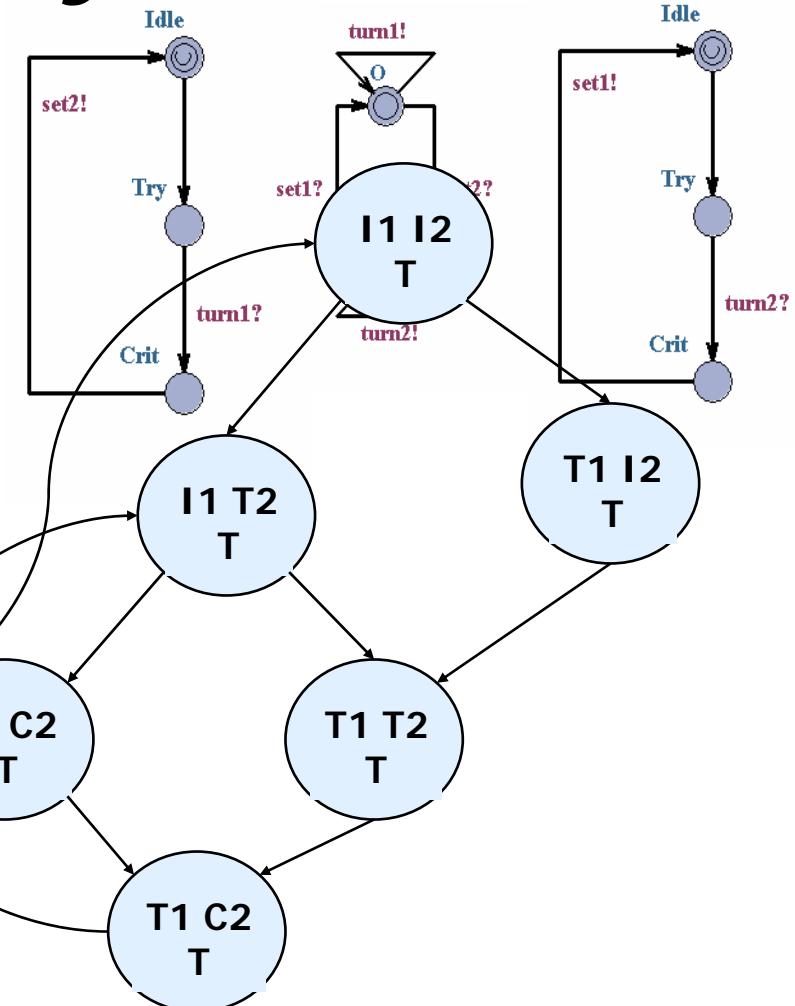
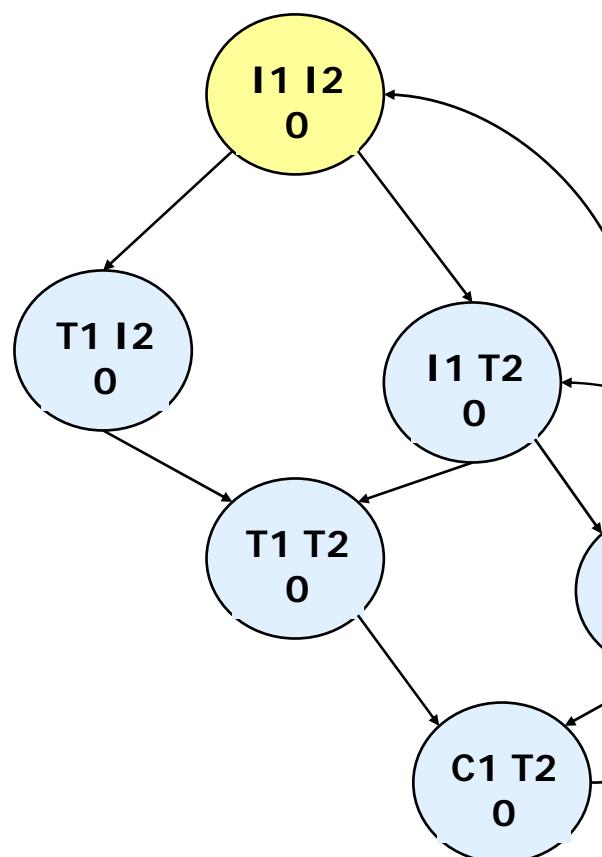


Turn

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Gensidig udelukkelse

Forward Reachability

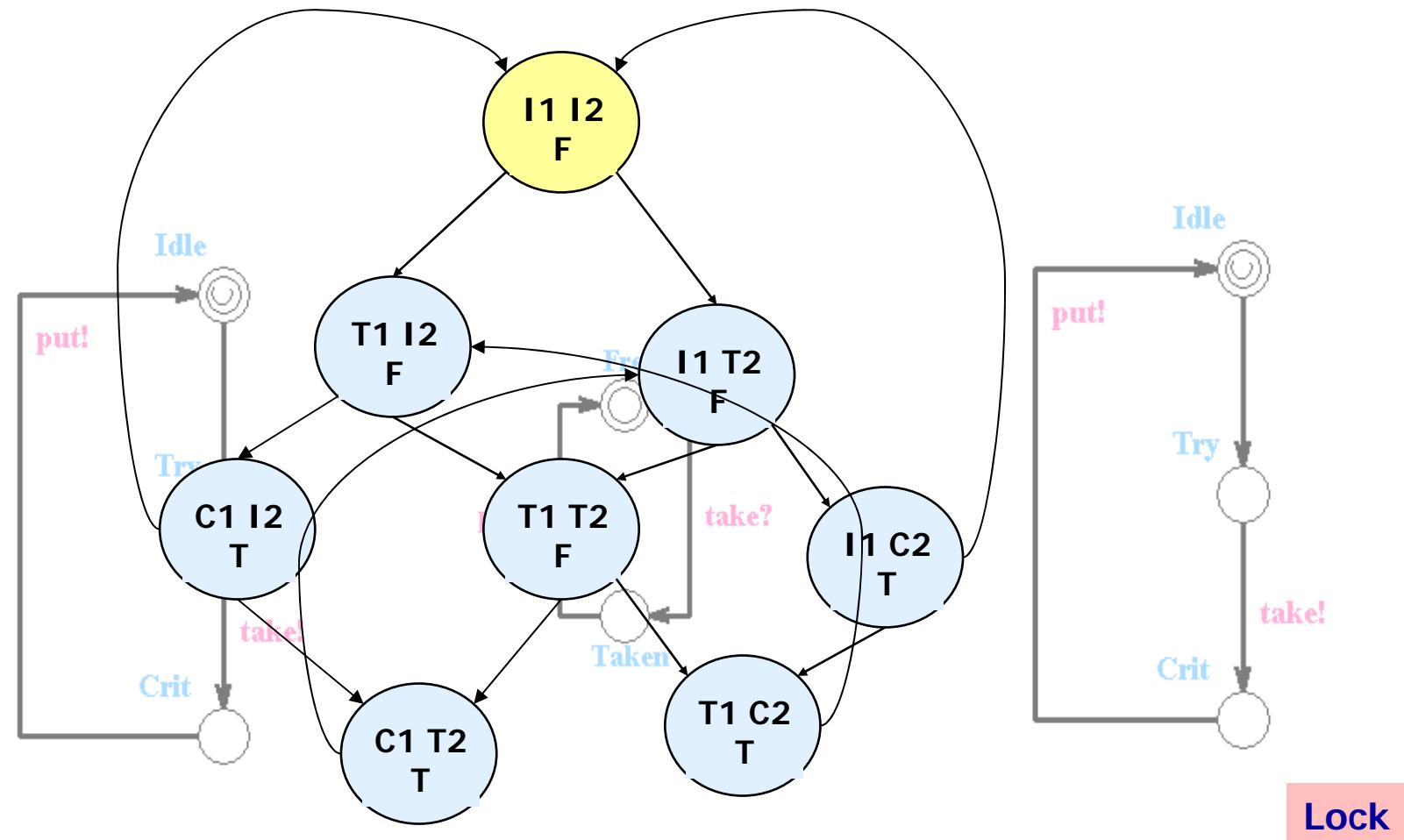


Turn

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Gensidig udelukkelse

Forward Reachability



CISS

Generiske egenskaber

- Non-determinisme
- Tilstande der ikke aktiveres
- Transitioner der ikke bruges
- Input der ikke processeres
- Output der ikke genereres
- Lokal deadlock
- System deadlock

Kan alle reduceres til
REACHABILITY

Train Simulator

VVS
visualSTATE

1421 machines

11102 transitions

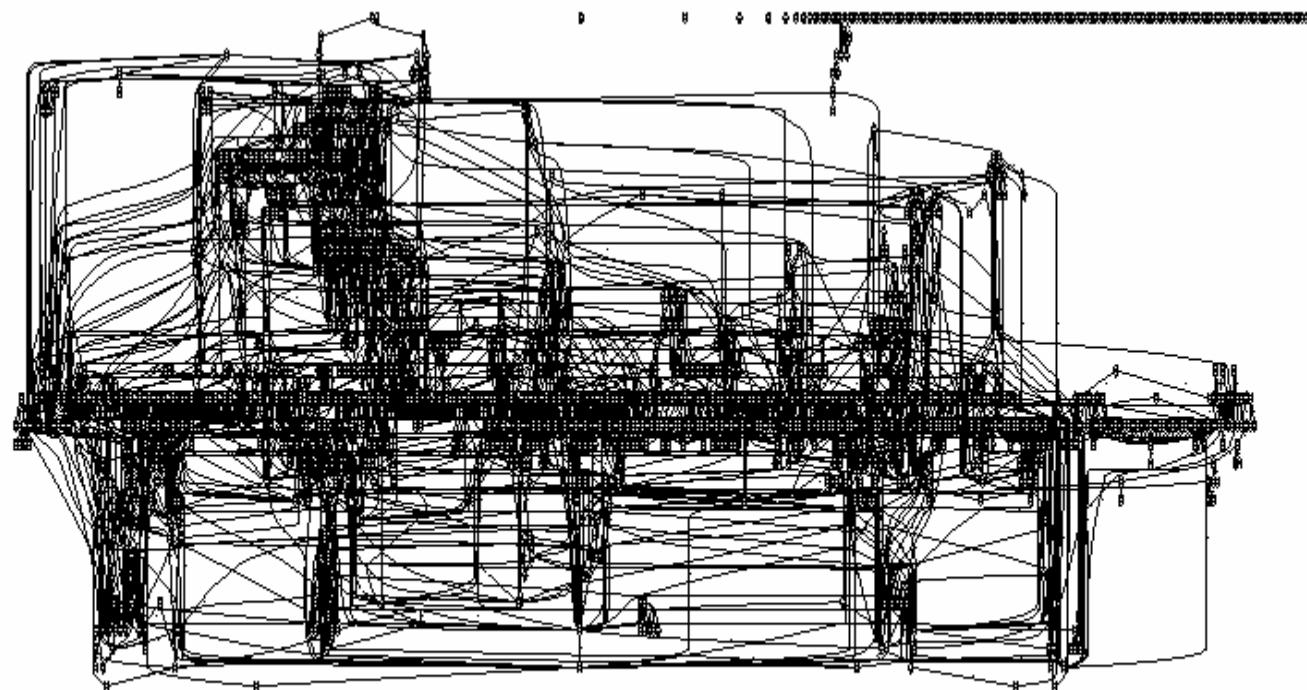
2981 inputs

2667 outputs

3204 local states

Declare state sp.: 10^{476}

BUGS ?



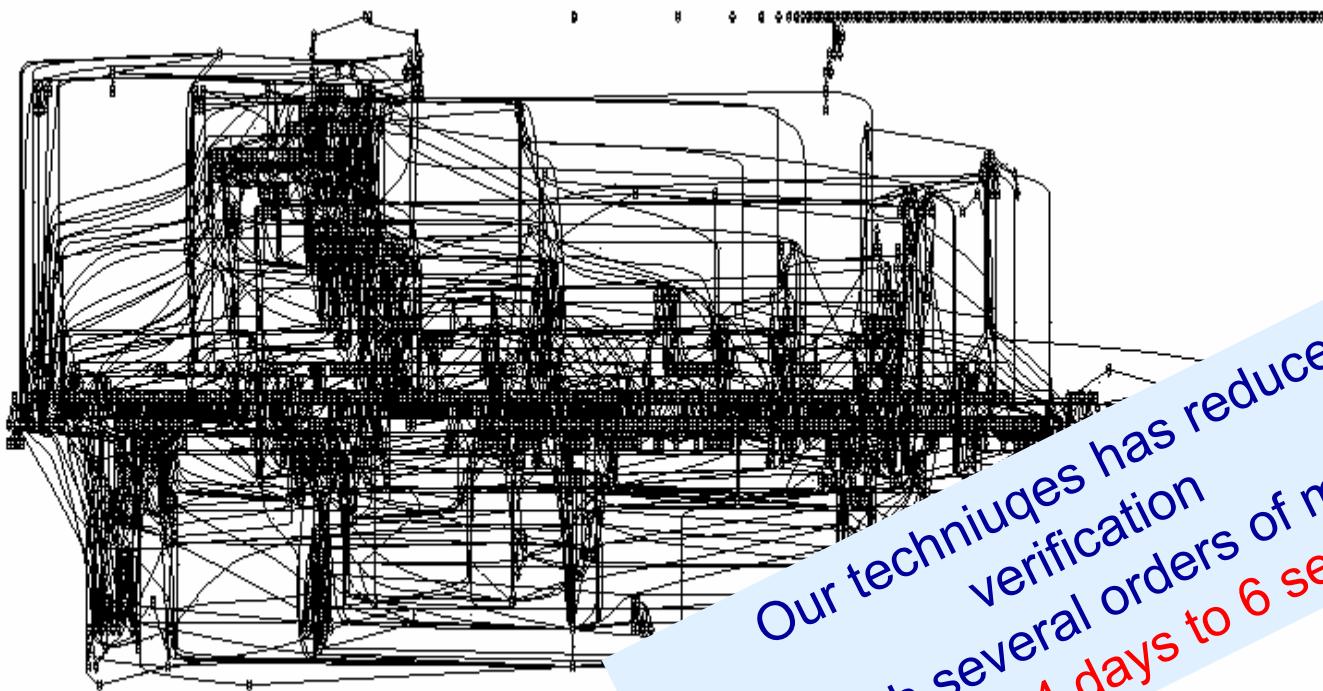
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Train Simulator

VVS
visualSTATE

1421 machines
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BUGS ?



Our techniques has reduced
time with several orders of magnitude
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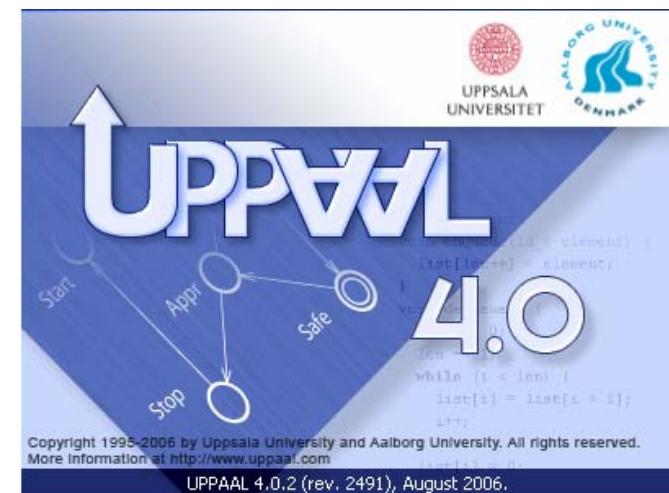
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Adding Time

FSM



Timed Automata



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Collaborators

@AALborg

- Kim G Larsen
- Gerd Behrman
- Arne Skou
- Brian Nielsen
- Alexandre David
- Jacob Illum Rasmussen
- Marius Mikucionis

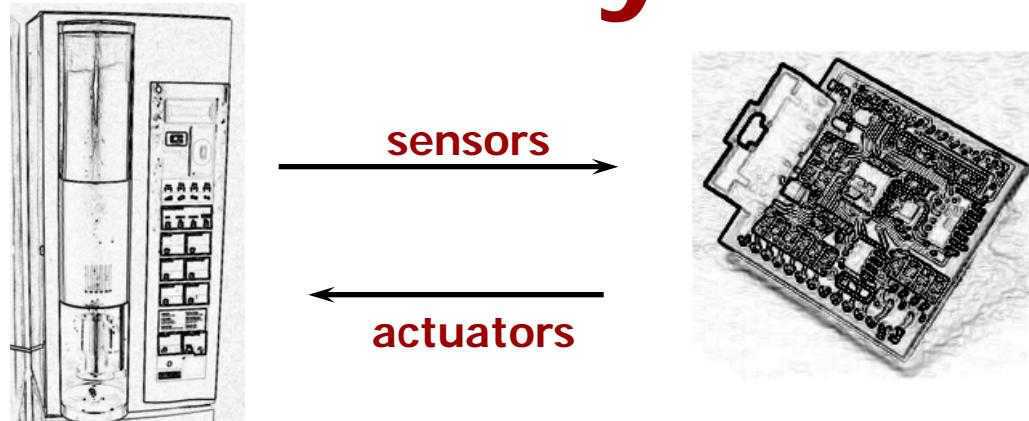
@UPPsala

- Wang Yi
- Paul Pettersson
- John Håkansson
- Anders Hessel
- Pavel Krcal
- Leonid Mokrushin
- Shi Xiaochun

@Elsewhere

- Emmanuel Fleury, Didier Lime, Johan Bengtsson, Fredrik Larsson, Kåre J Kristoffersen, Tobias Amnell, Thomas Hune, Oliver Möller, Elena Fersman, Carsten Weise, David Griffioen, Ansgar Fehnker, Frits Vandraager, Theo Ruys, Pedro D'Argenio, J-P Katoen, Jan Tretmans, Judi Romijn, Ed Brinksma, Martijn Hendriks, Klaus Havelund, Franck Cassez, Magnus Lindahl, Francois Laroussinie, Patricia Bouyer, Augusto Burgueno, H. Bowmann, D. Latella, M. Massink, G. Faconti, Kristina Lundqvist, Lars Asplund, Justin Pearson...

Real Time Systems



Plant
Continuous

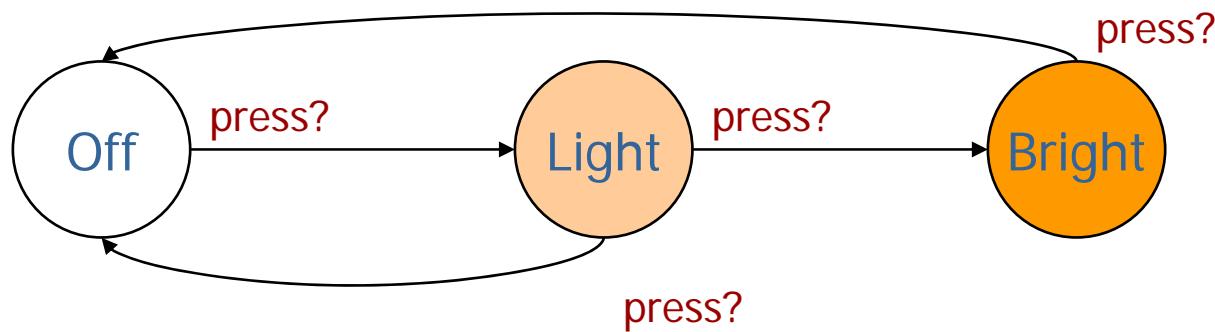
Controller Program
Discrete

Eg.: Realtime Protocols
Pump Control
Air Bags
Robots
Cruise Control
ABS
CD Players
Production Lines

Real Time System

A system where correctness not only depends on the logical order of events but also on their **timing!!**

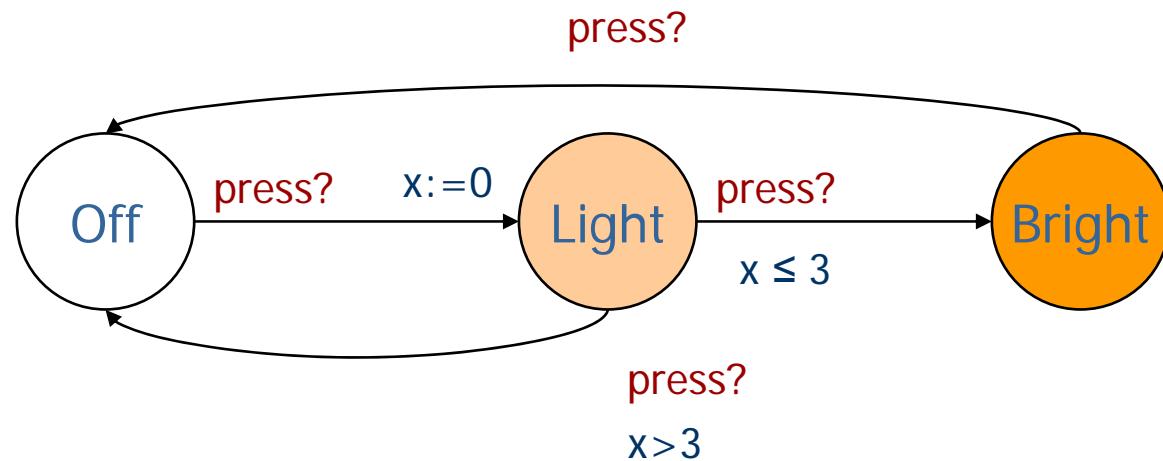
Dumb Light Control



WANT: if **press** is issued twice **quickly**
then the **light** will get **brighter**; otherwise the light is
turned **off**.

Dumb Light Control

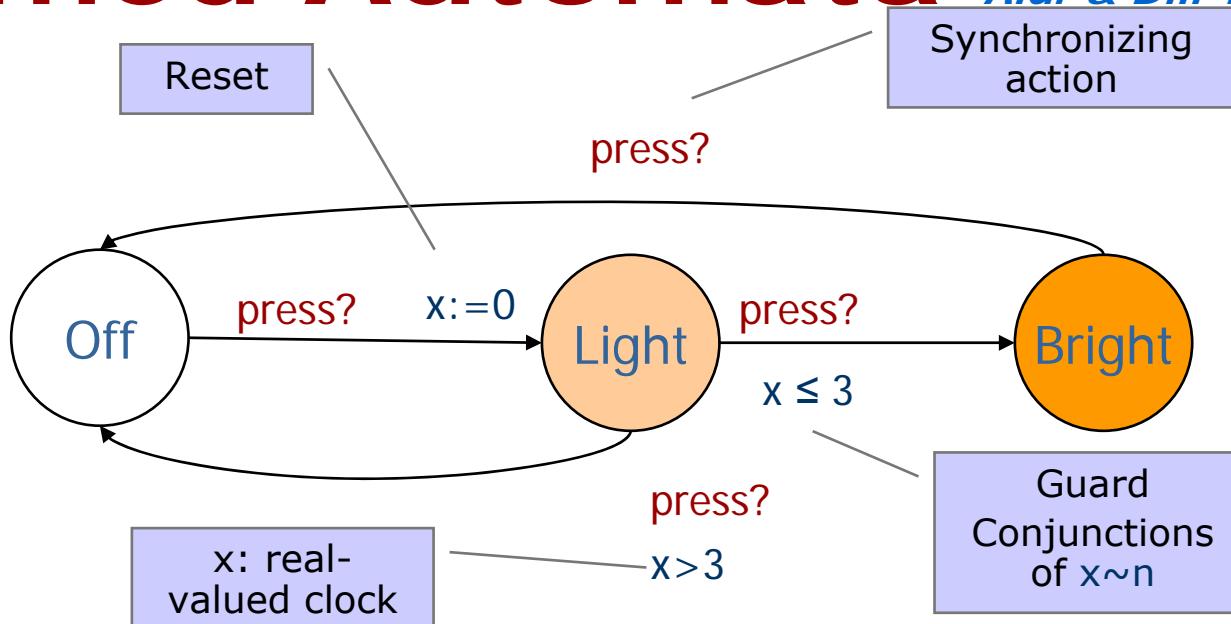
Alur & Dill 1990



Solution: Add real-valued clock x

Timed Automata

Alur & Dill 1990



States:

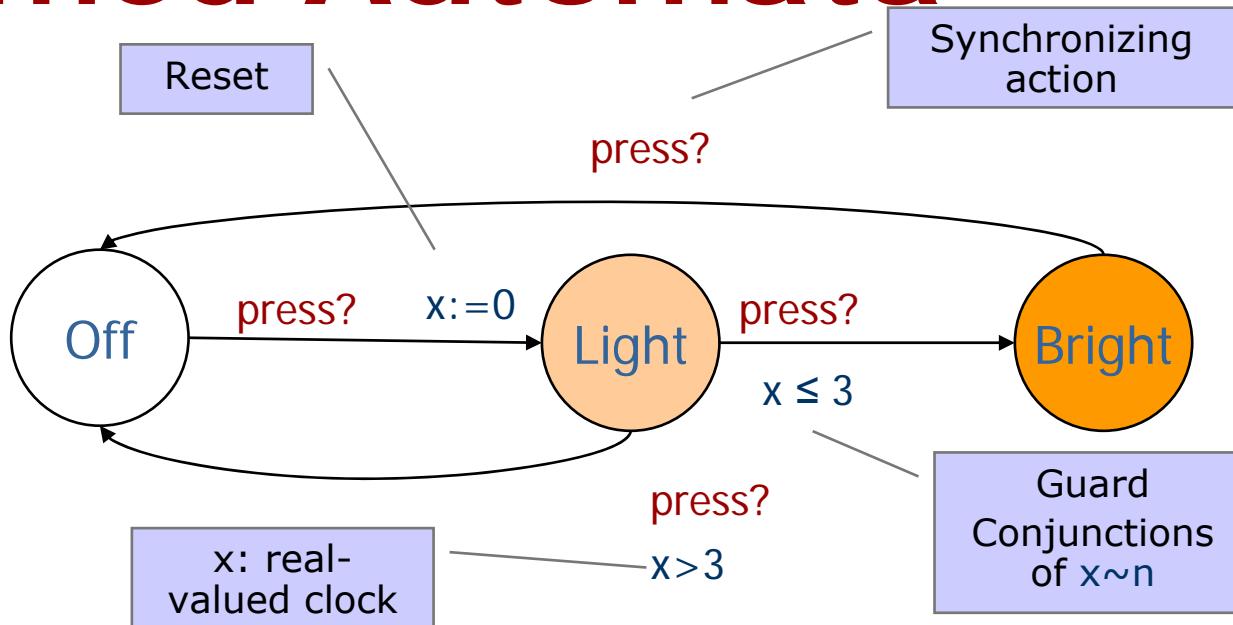
(location , $x=v$) where $v \in \mathbb{R}$

Transitions:

(Off , $x=0$)

Timed Automata

Alur & Dill 1990



States:

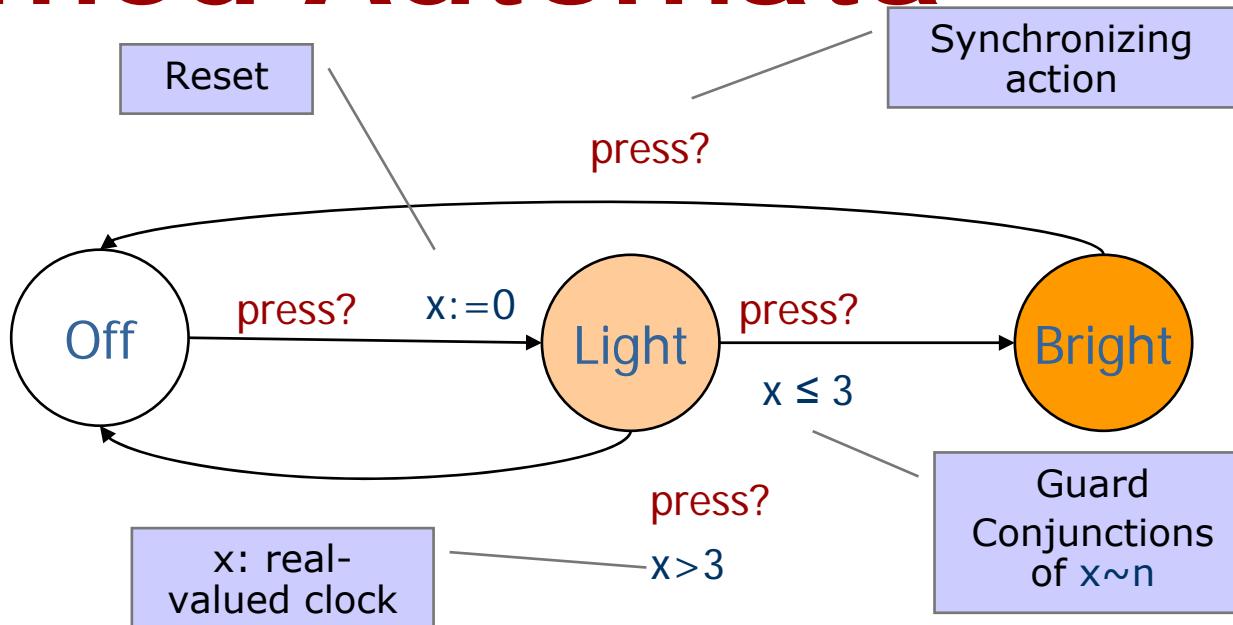
(location , $x=v$) where $v \in \mathbb{R}$

Transitions:

(Off , $x=0$)
delay 4.32 → (Off , $x=4.32$)

Timed Automata

Alur & Dill 1990



States:

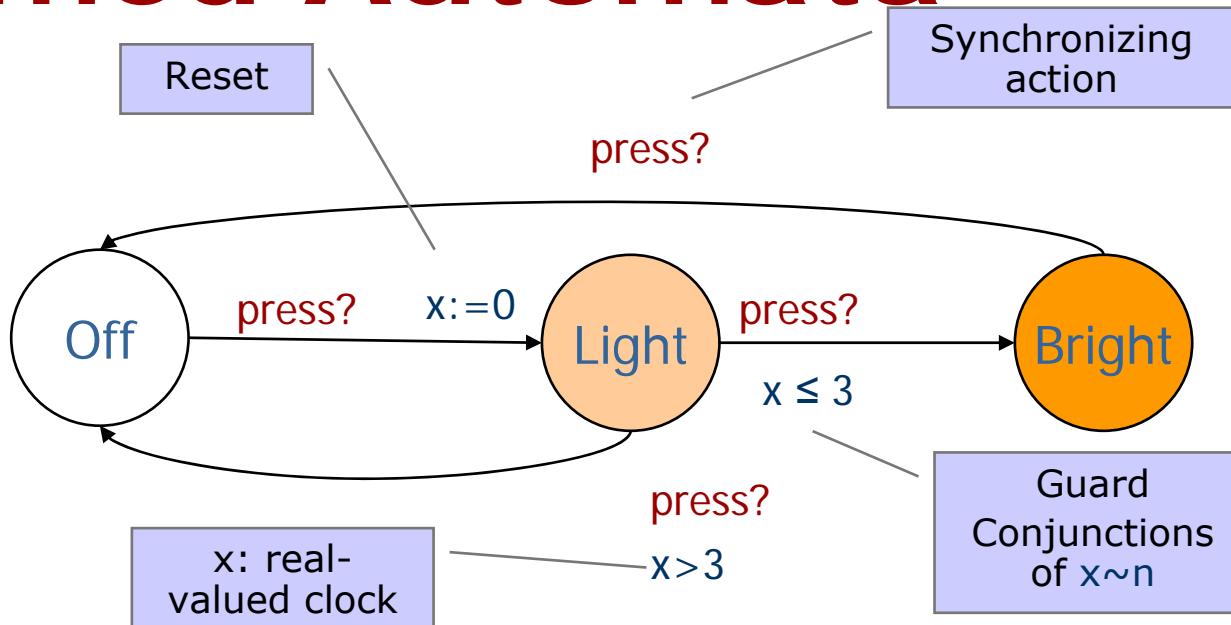
(location , $x=v$) where $v \in \mathbb{R}$

Transitions:

delay 4.32 → (Off , $x=4.32$)
press? → (Light , $x=0$)

Timed Automata

Alur & Dill 1990



States:

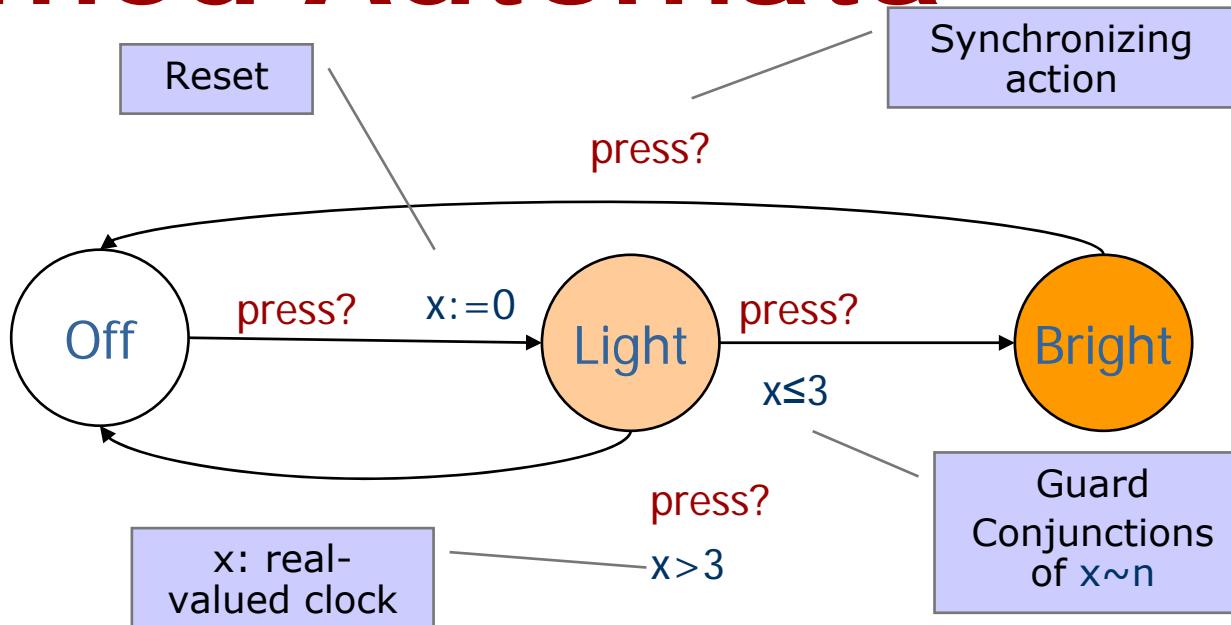
(location , $x=v$) where $v \in \mathbb{R}$

Transitions:

(Off , $x=0$)
delay 4.32 → (Off , $x=4.32$)
press? → (Light , $x=0$)
delay 2.51 → (Light , $x=2.51$)

Timed Automata

Alur & Dill 1990



States:

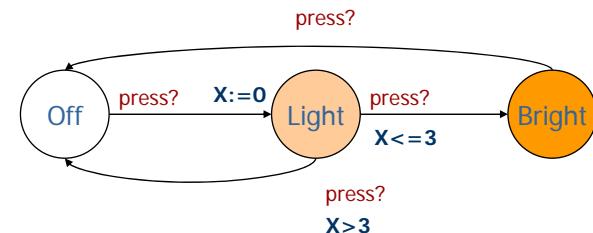
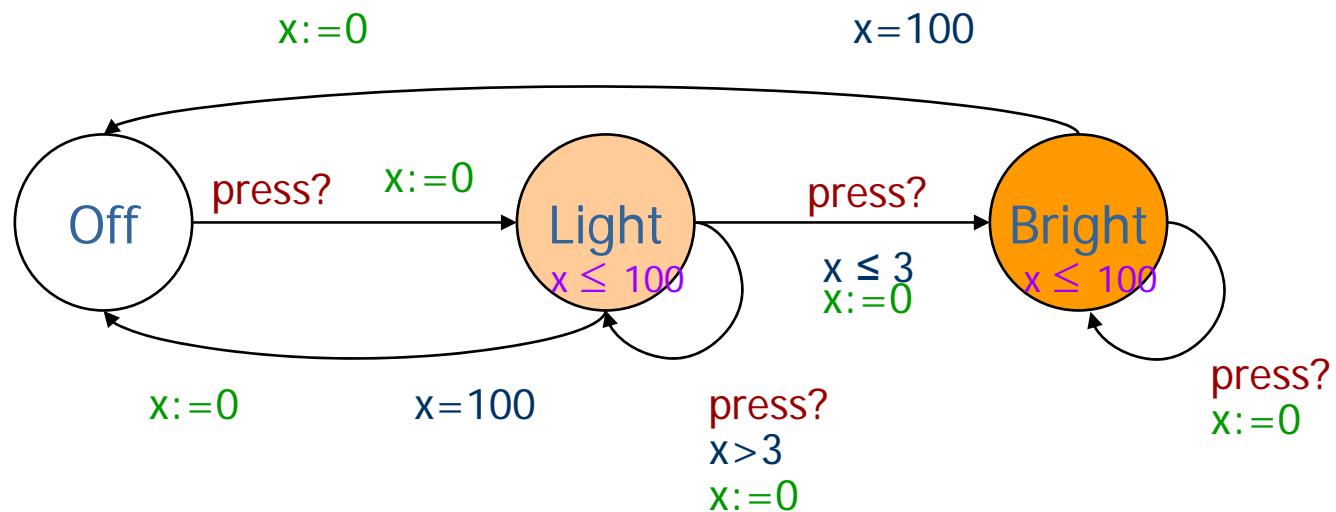
(location , $x=v$) where $v \in \mathbb{R}$

Transitions:

- | | | |
|------------|---------------|-----------------------|
| delay 4.32 | \rightarrow | (Off , $x=4.32$) |
| press? | \rightarrow | (Light , $x=0$) |
| delay 2.51 | \rightarrow | (Light , $x=2.51$) |
| press? | \rightarrow | (Bright , $x=2.51$) |

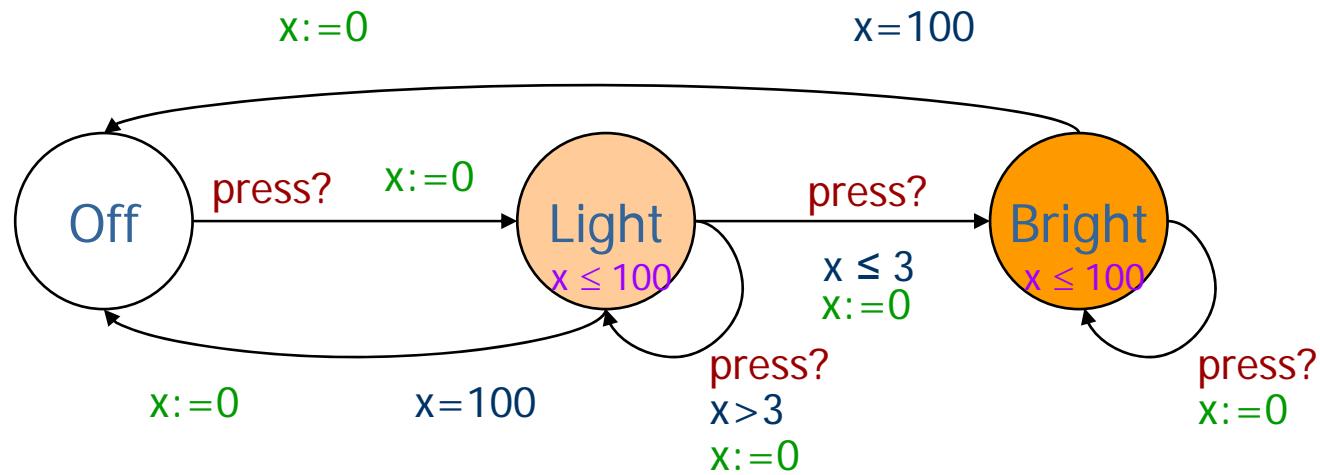
Intelligent Light Control

Using Invariants



Intelligent Light Control

Using Invariants



Transitions:

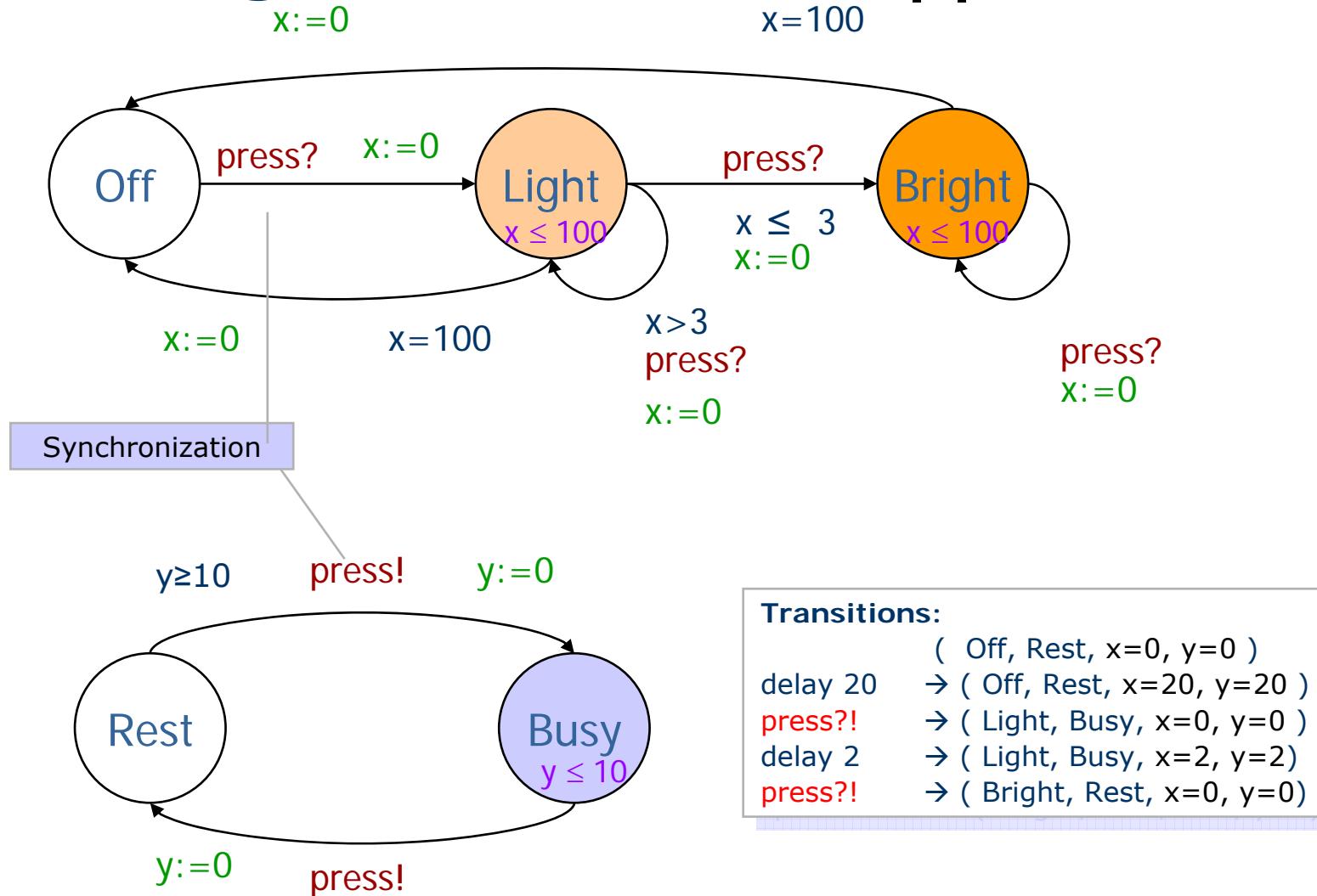
delay 4.32	(Off , x=0) → (Off , x=4.32)
press?	→ (Light , x=0)
delay 4.51	→ (Light , x=4.51)
press?	→ (Light , x=0)
delay 100	→ (Light , x=100)
τ	→ (Off , x=0)

Note:

(Light , x=0) delay 103 → X

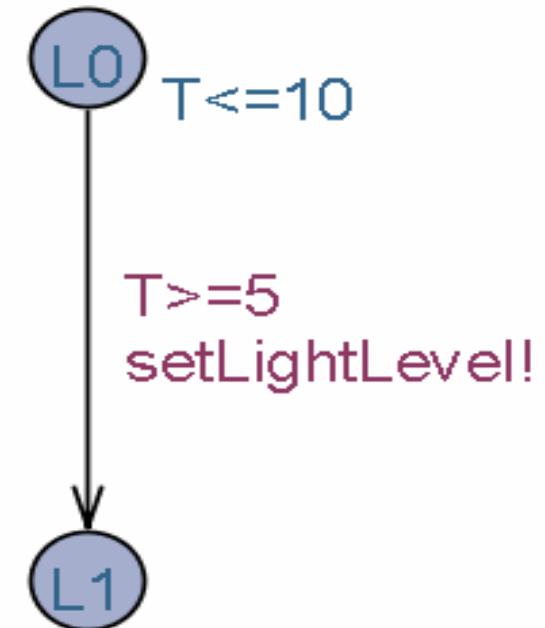
Invariants ensures progress

Light Controller || User



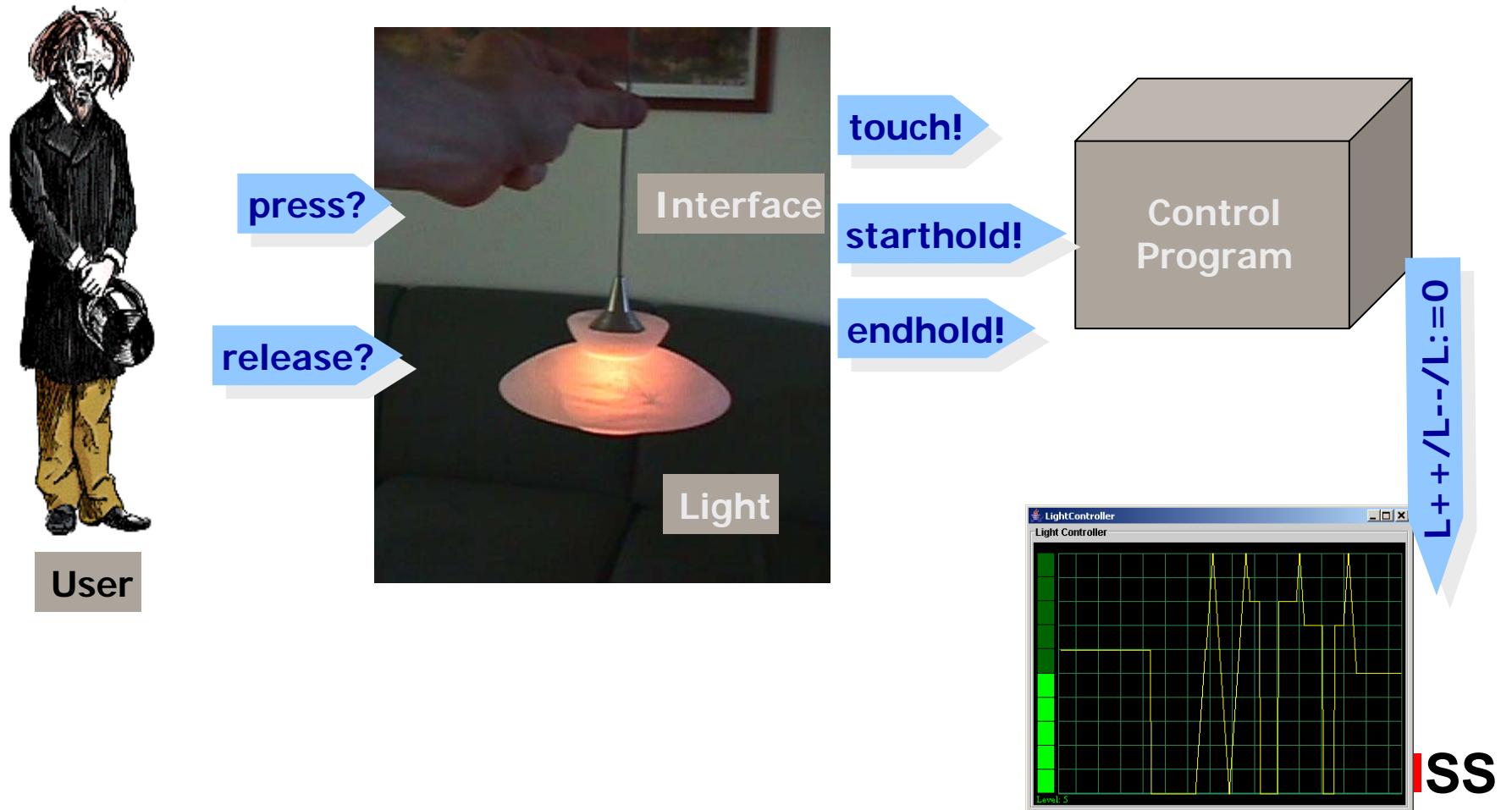
Timing Uncertainty

- Unpredictable or variable
 - ✿ response time,
 - ✿ computation time
 - ✿ transmission time etc:
- Initially $T=0$

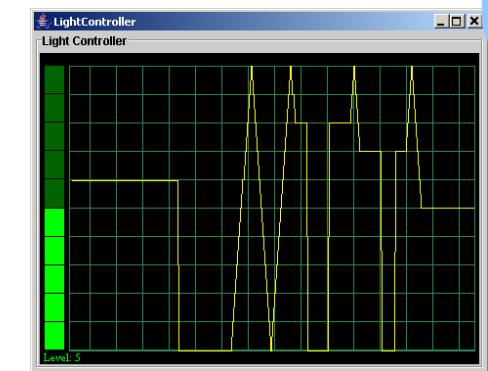
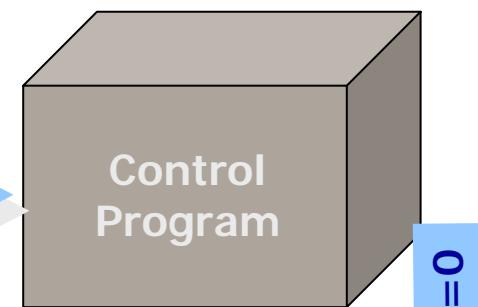
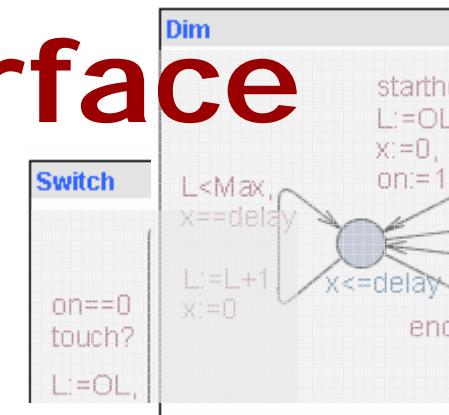
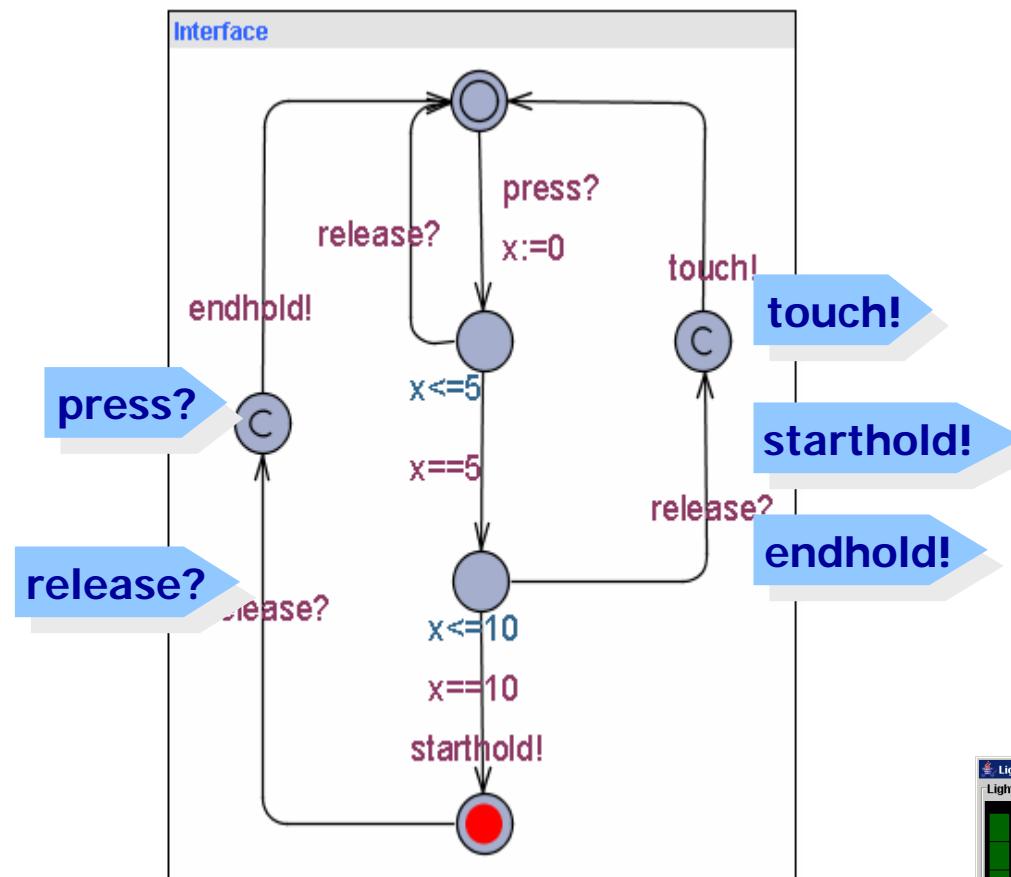


LightLevel must be adjusted between 5 and 10

Light Control Interface



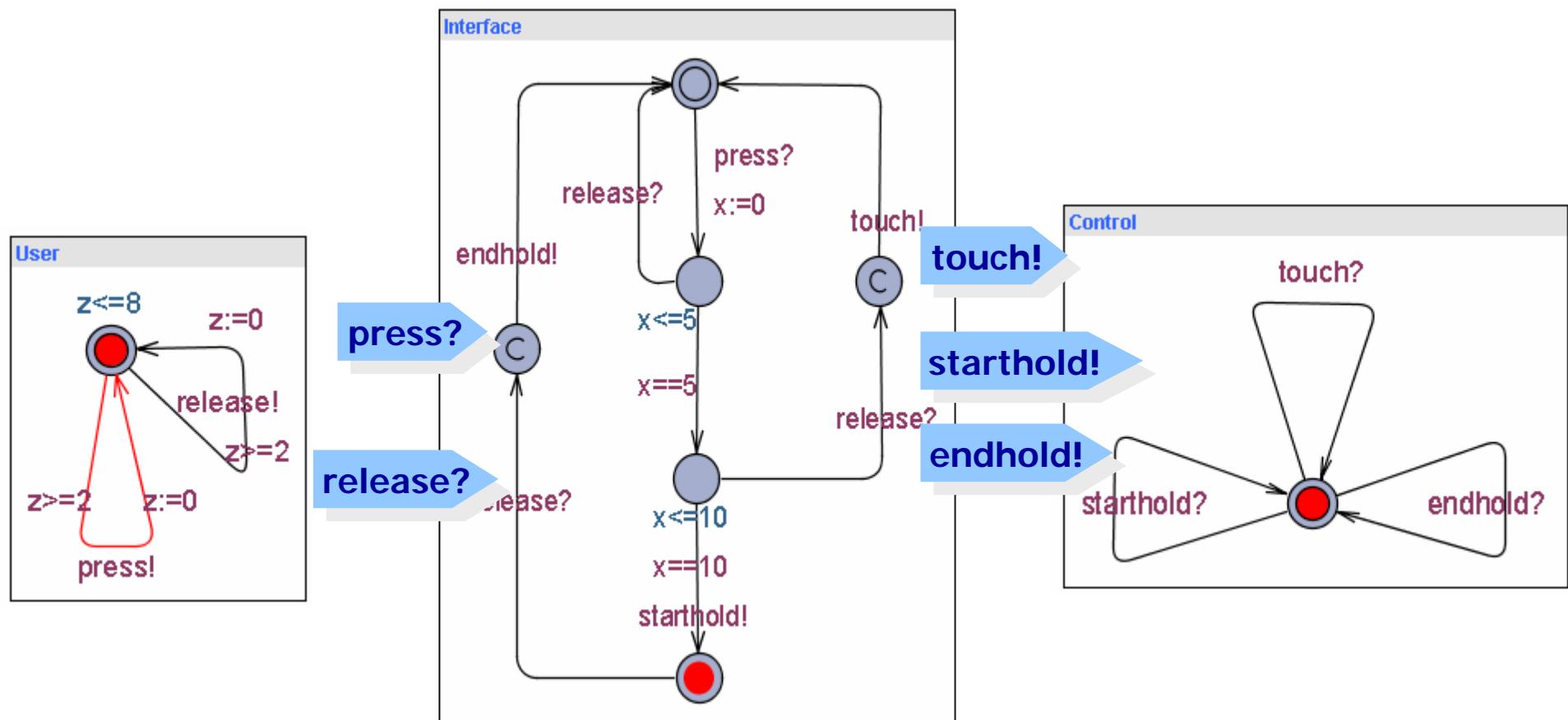
Light Control Interface



L₊₊/L₋₋/L_{:=}=0

ISS

Light Control Network

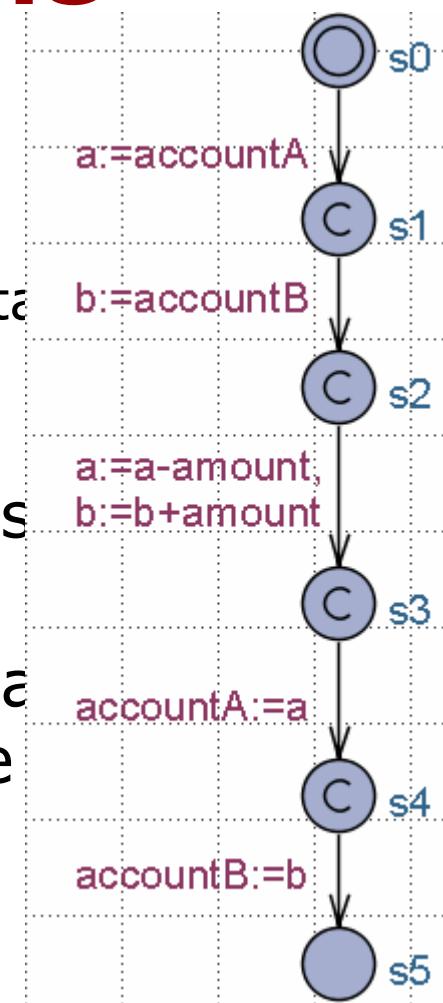


Broad-casts

- chan coin, cof, cofBut;
- broadcast chan join;
 - sending: output join!
 - every automaton that listens to join moves
 - ie. every automaton with enabled “join?” transition moves in one step
 - may be zero!

Committed Locations

- Locations marked **C**
 - * **No delay** in committed location.
 - * Next transition must involve automata in ***committed location***.
- Handy to model atomic sequences
- The use of committed locations reduces the number of states in a model, and allows for more space and time efficient analysis.
- S0 to s5 executed atomically



Urgent Channels and Locations

- Locations marked **U**
 - ✿ *No delay* in committed location.
 - ✿ Interleaving permitted
- Channels declared “**urgent chan**”
 - ✿ Time doesn’t elapse when a synchronization is possible on a pair of urgent channels
 - ✿ Interleaving allowed

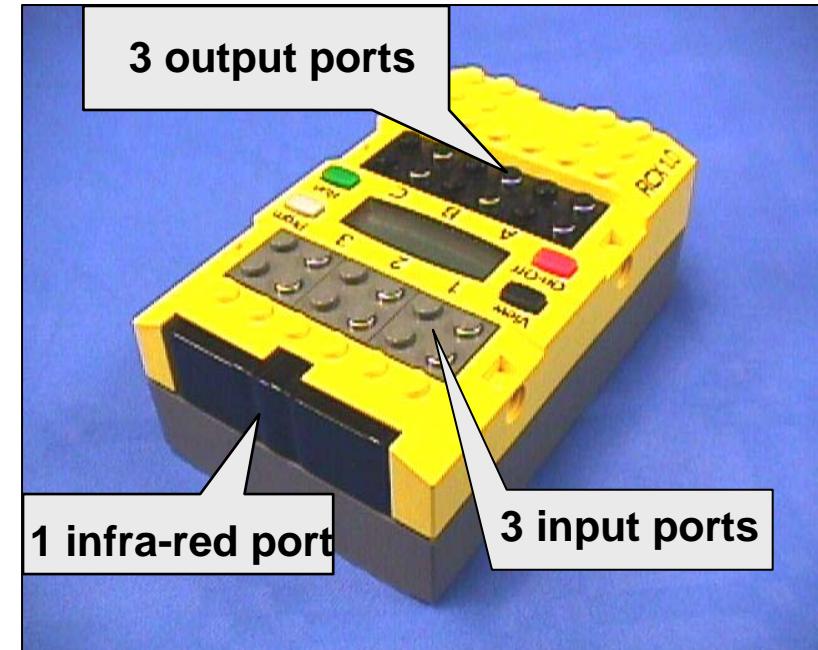
Other Uppaal features

- Bounded domain
 - Int [1..4] a;
- C-like data-structures and user defined functions in declaration section
 - structs, arrays, and typedef
- **select a:T construct**
- Forall, exists in expr
- Scalar sets (for giving unique ID's)
- Process and channel **priorities**
- Value passing (emulation)

BRICK SORTING

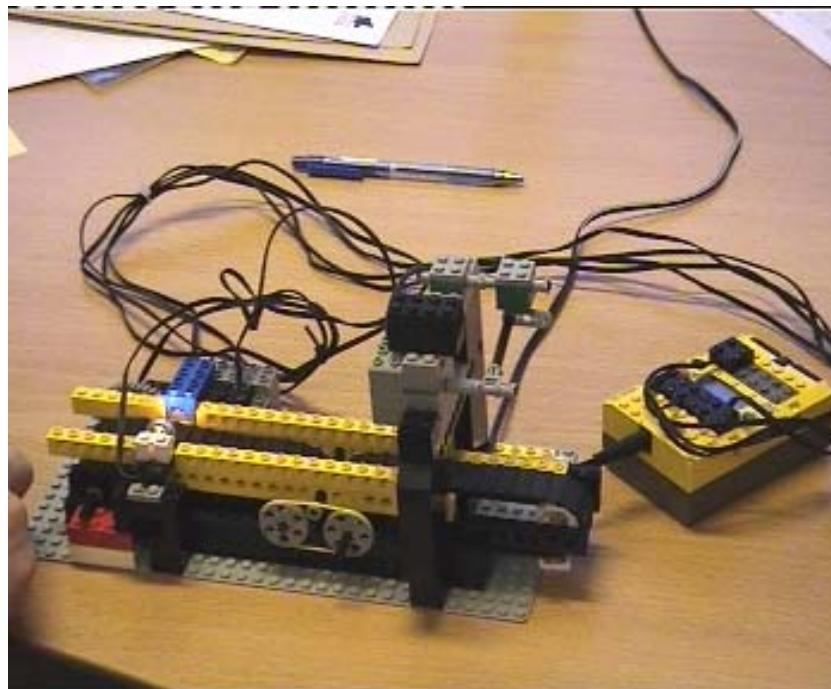
LEGO Mindstorms/RCX

- Sensors: temperature, light, rotation, pressure.
- Actuators: motors, lamps,
- Virtual machine:
 - * 10 tasks, 4 timers, 16 integers.
- Several Programming Languages:
 - * NotQuiteC, Mindstorm, Robotics, legOS, etc.



A Real Timed System

The Plant
Conveyor Belt
&
Bricks



**Controller
Program**
LEGO MINDSTORM

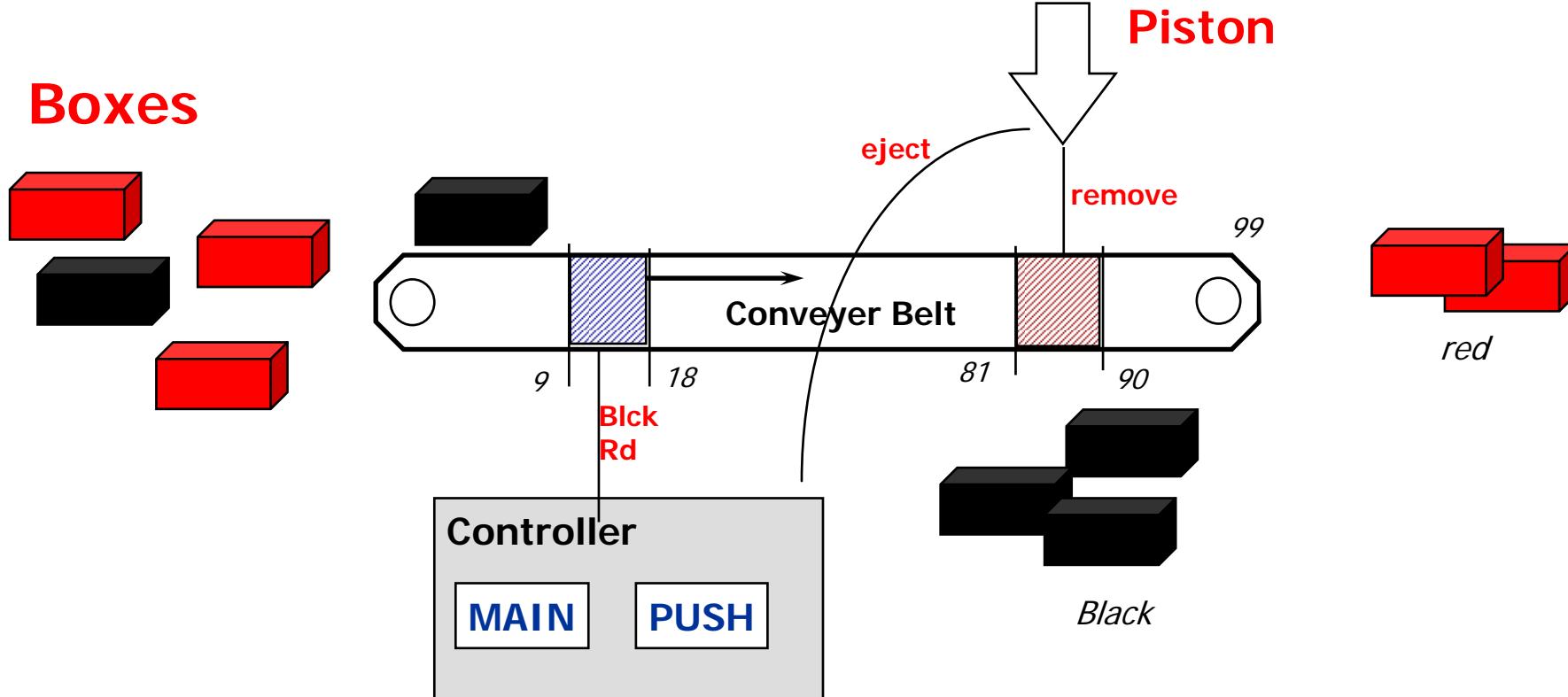
What is suppose to happen?

CISS

First UPPAAL model

Sorting of Lego Boxes

Ken Tindell



Exercise: Design **Controller** so that only black boxes are being pushed out

NQC programs

```
int active;
int DELAY;
int LIGHT_LEVEL;
```

```
task MAIN{
    DELAY=75;
    LIGHT_LEVEL=35;
    active=0;
    Sensor(IN_1, IN_LIGHT);
    Fwd(OUT_A,1);
    Display(1);

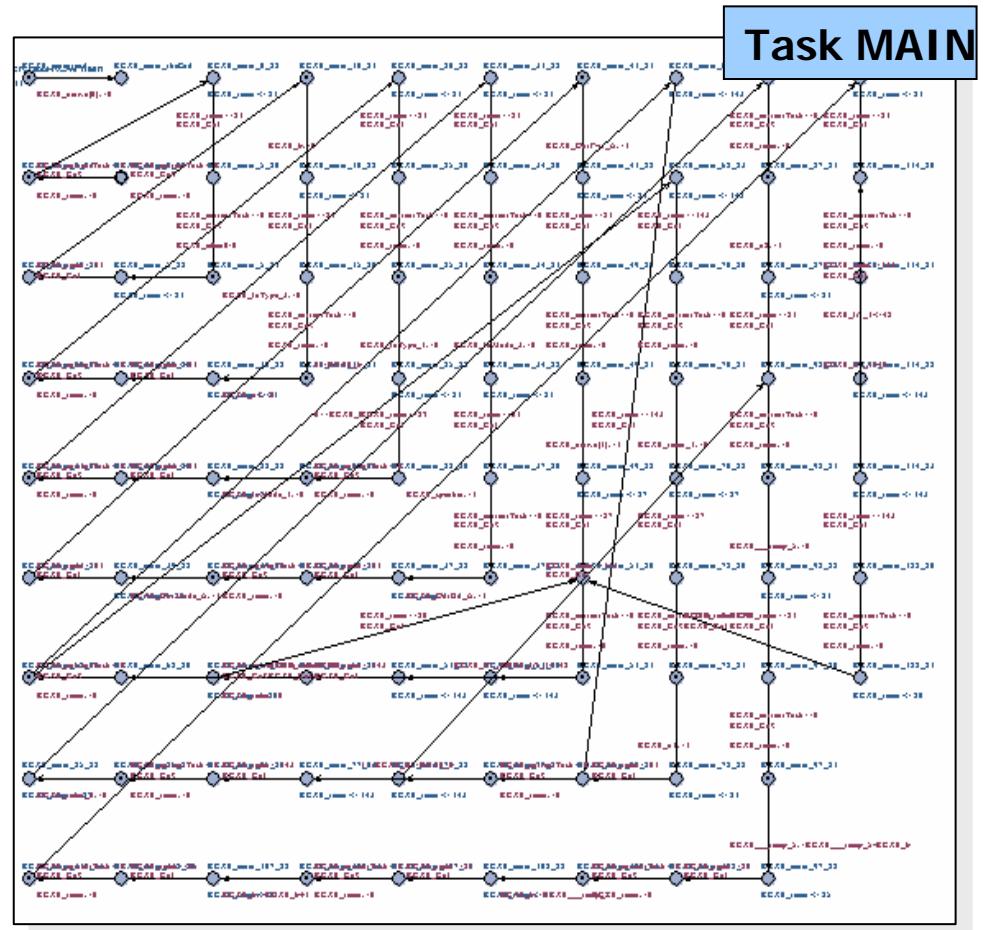
    start PUSH;

    while(true){
        wait(IN_1<=LIGHT_LEVEL);
        ClearTimer(1);
        active=1;
        PlaySound(1);
        wait(IN_1>LIGHT_LEVEL);
    }
}
```

```
task PUSH{
    while(true){
        wait(Timer(1)>DELAY && active==1);
        active=0;
        Rev(OUT_C,1);
        Sleep(8);
        Fwd(OUT_C,1);
        Sleep(12);
        Off(OUT_C);
    }
}
```

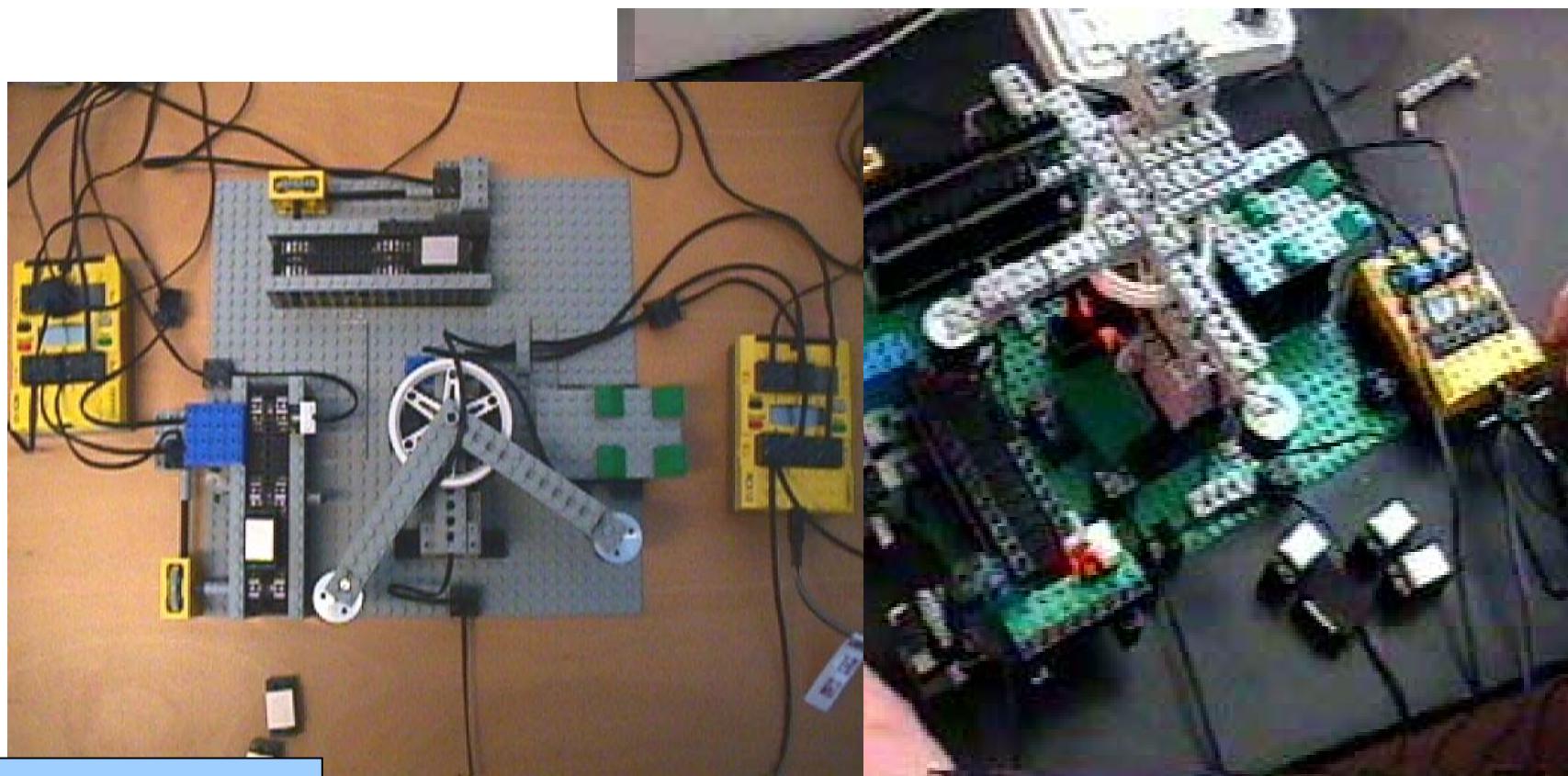
From RCX to UPPAAL

- Model includes Round-Robin Scheduler.
- Compilation of RCX tasks into TA models.
- Presented at ECRTS 2000



The Production Cell

Course at DTU, Copenhagen



Production Cell