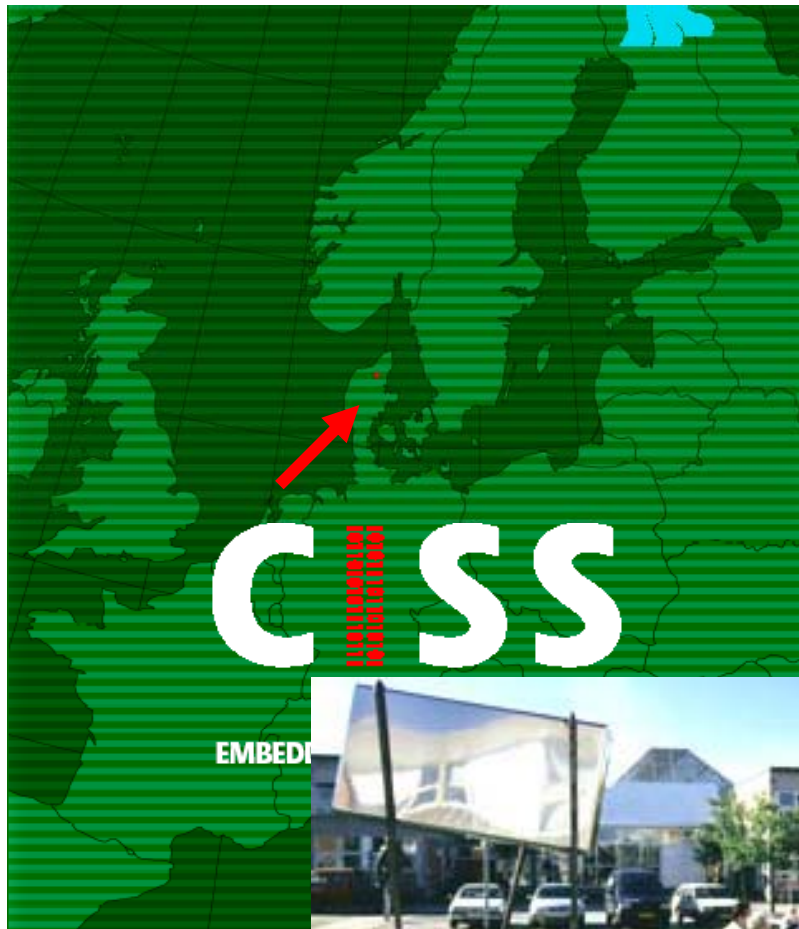


Validation, Synthesis and Performance Evaluation of Embedded Systems — using UPPAAL —

Kim Guldstrand Larsen



CISS: *Center for Embedded Software Systems*



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or

CISS

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96357220

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Fr. Bajersvej 7B
9220 Aalborg Ø

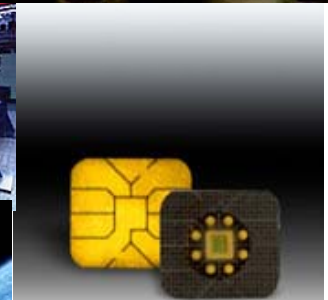
Aalborg



Aalborg University leading Danish ICT University in terms of public investments (33%)

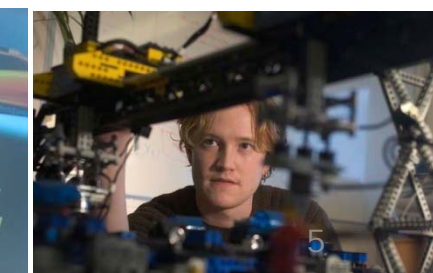
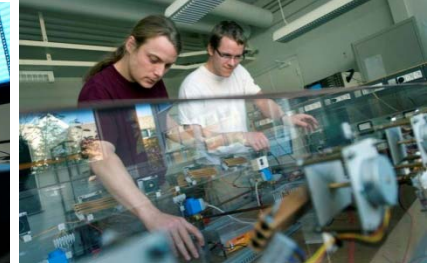
Why CISS

- 80% of all software is embedded
- Demands for **increased functionality** with **minimal resources**
- Requires multitude of skills
 - Software construction
 - Hardware platforms
 - Communication
 - Automation
- **Goal:**
Give a qualitative lift to current industrial practice
!!!!!!



CISS in Numbers

- National Competence Center (2003-...)
 - Ministry of Tech. & Res.
 - North Jutland
 - Aalborg City
 - Aalborg University
- 50 Industrial Projects
- 20 CISS employees
- 25 CISS ass. Res.
- 20 Industrial PhDs
- 10 Elite Students
- 10 MEUR

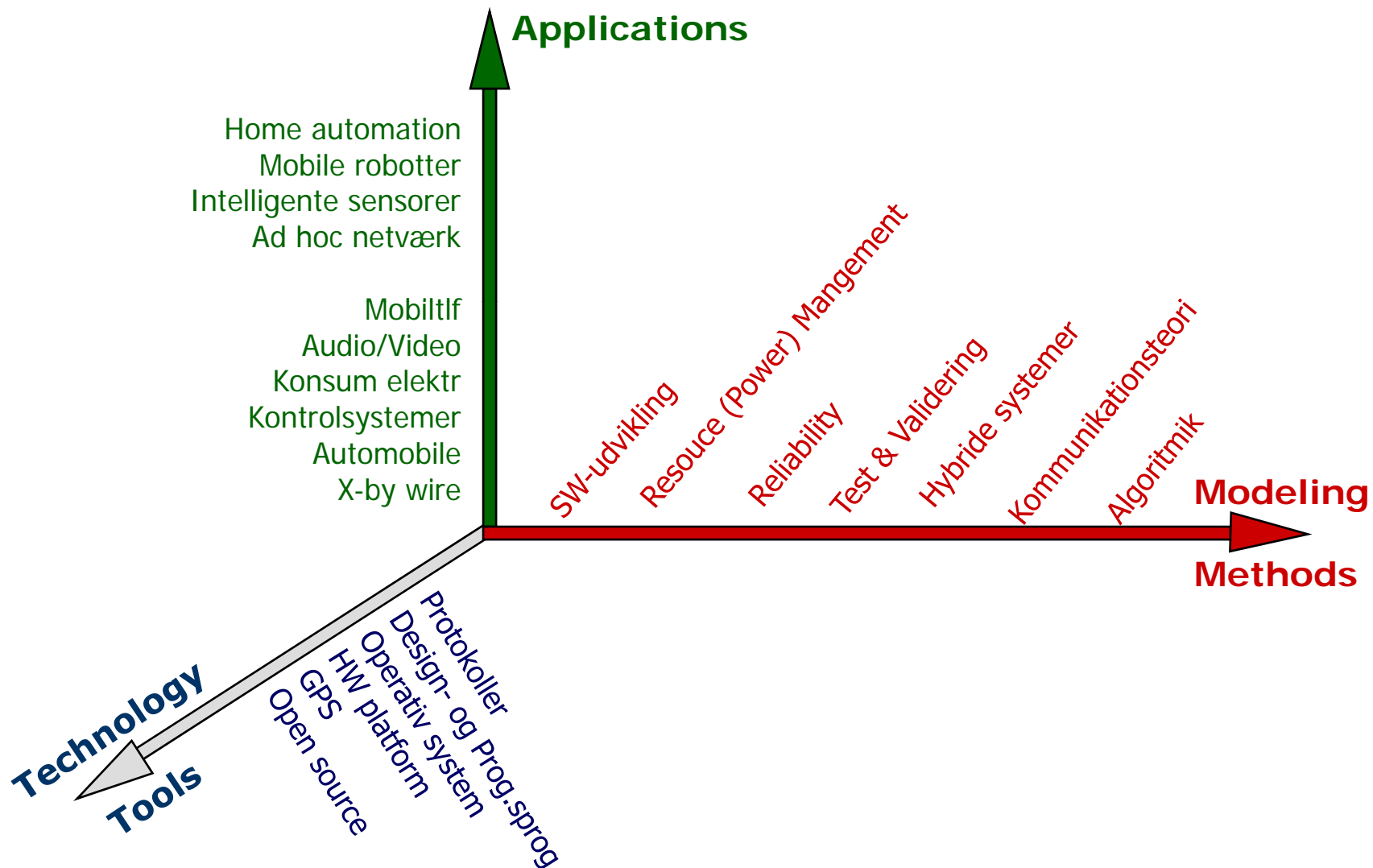


Partners

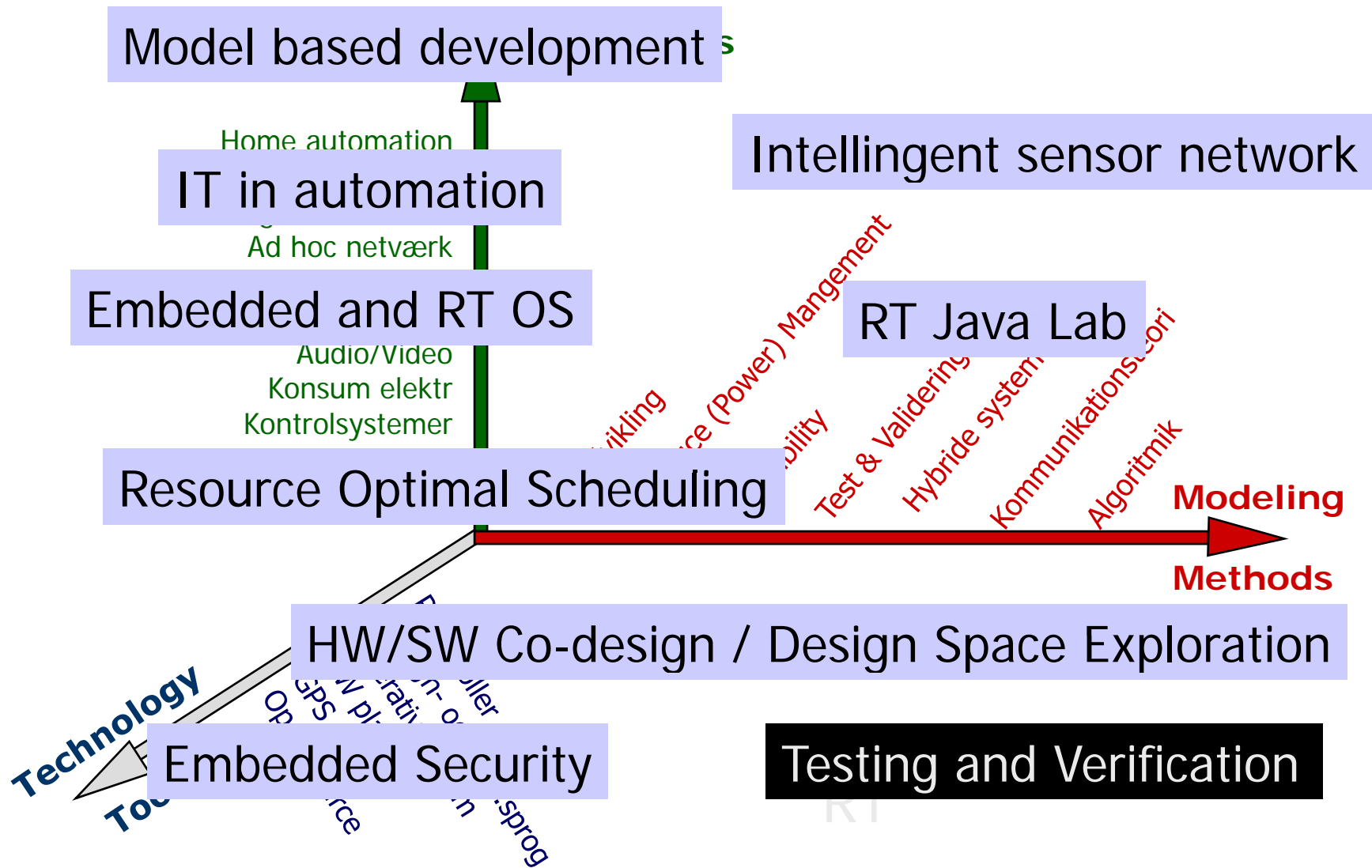
- Aeromark
- Analog Devices
- Blip Systems
- Danfoss
- Ericsson Telebit
- ETI
- Exhausto
- FOSS
- GateHouse
- Grundfos
- IAR Systems
- MAN B&W
- Novo Nordisk
- Motorola
- Panasonic
- RTX Telecom
- S-Card
- Simrad
- Skov
- SpaceCom
- TK Systemtest
- TDC Totalløsninger
- Aalborg Industries
- LandsCentret

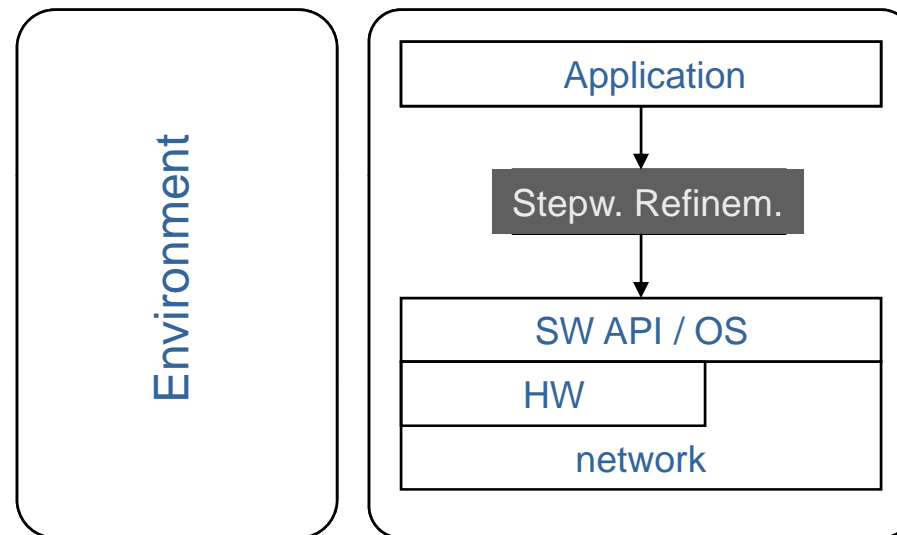


Focus Areas



Focus Areas





Funded by Danish Advanced Technology Foundation
Budget 9 MEuro / 4 years



DaNES

Danish Network for Intelligent Embedded Systems

Challenges

Selfdiagnostic & -repair



Test & Verificaiton

**Model Driven
and
Component Based
Development**



Embedded & Distributed



Informatik og Matematisk Modellering

Platform



Development

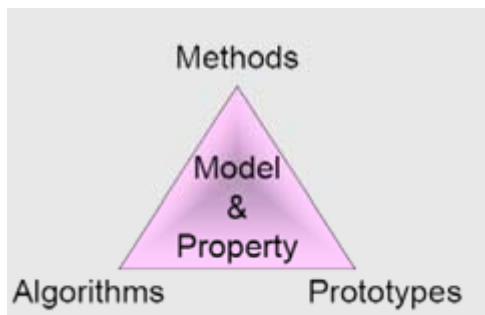


MT LAB Modelling of Information Technology

Villum-Kahn Rasmussen Center of Excellence

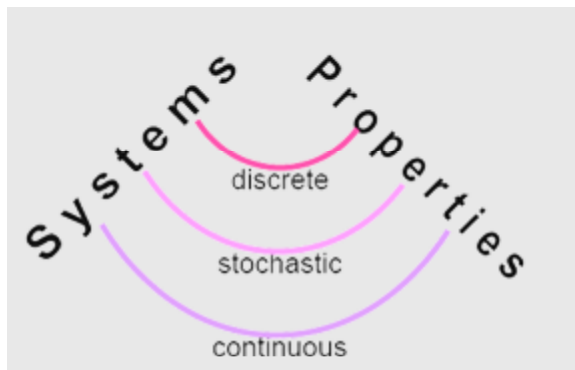
Opening November 19, 2008

6.5 MEUR



Static Analysis

Model Checking



Embedded Systems



Service Oriented Architectures

IMM/DTU, CISS/AAU, ITU

Director Flemming Nielson

Co-Director Kim G Larsen

IDEA⁴CPS



Foundations for Cyber-Physical Systems

❖ From Computer Science to Cyber Physical Systems



MT-LAB Meeting 11.1.2011

Kim Guldstrand Larsen [6]



❖ Topics & Task Overview



- Specification and Modeling
- Validation and Analysis
- Compositionality versus Global Features
- Cross-Level Preservation
- Mini Cases
- Prototype Tools

MT-LAB Meeting 11.1.2011

Kim Guldstrand Larsen [17]



IDEA⁴CPS



Foundations for Cyber-Physical Systems

❖ From Computer Science to
Cyber Physical Systems



MT-LAB Meeting 11.1.2011



W

Modeling

Analysis

versus Global

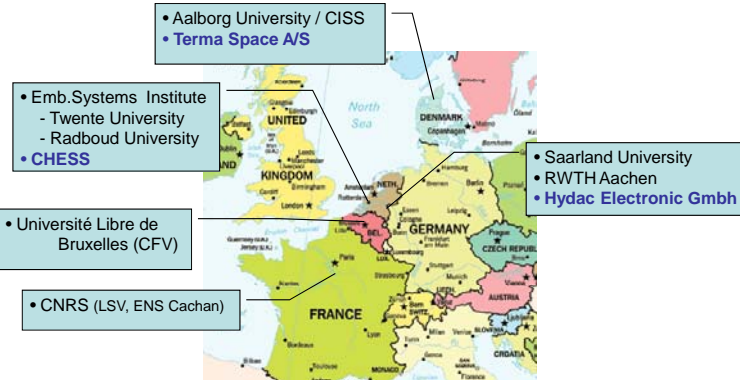
ervation



Kim G Larsen [17]

Quasimodo

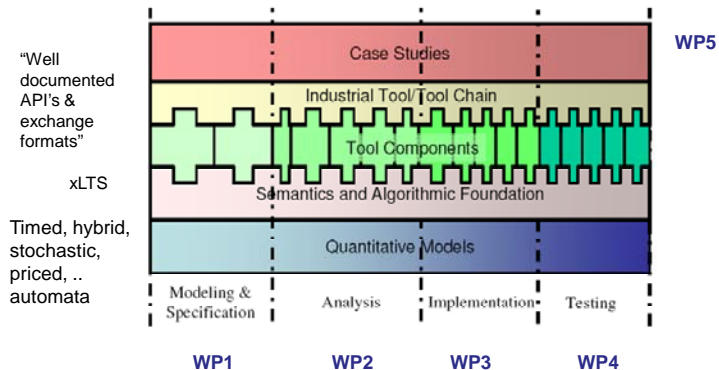
Partners



Quasimodo, ESWEEK, Scottsdale, October 24, 2010

Page 2

Workplan Strategy



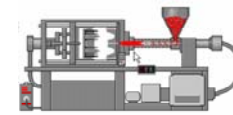
Quasimodo, ESWEEK, Scottsdale, October 24, 2010

Page 5

WP5 Case Studies



- **Accumulator Charge Controller (HYDAC)**
 - Design of robust and optimal control for hydraulic pump
 - (UPPAAL Tiga, Phaver, Simulink)
- **Wireless Sensor Network (CHES)**
 - Analysis of gMAC protocol (UPPAAL)
 - Potential of time synchronization failing Identified, demonstrated and partially corrected (UPPAAL)
 - Testing (jTorX, TorXakis, TRON)
 - Trade-off between energy consumption and collision rates (MODEST)
- **Control Software for satellites Hershel and Planck (TERMA)**
 - Schedulability and WCET analysis (UPPAAL)



Quasimodo, ESWEEK, Scottsdale, October 24, 2010

Page 6

WP5 Additional Case Studies



- **Self-Balancing Scooter (CHES)**
 - Highlevel control-modes modeled by engineers (UPPAAL)
 - Schedulability (UPPAAL)
- **Adaptive scheduling of data paths (OCE)**
 - Synthesis of optimal data path (CORA)
- **Rapid Input-Output Packet Switch (ASML)**
 - Simulation and verification of worst-case latencies (POOSL, UPPAAL)



Quasimodo, ESWEEK, Scottsdale, October 24, 2010

Page 7

Quasimodo



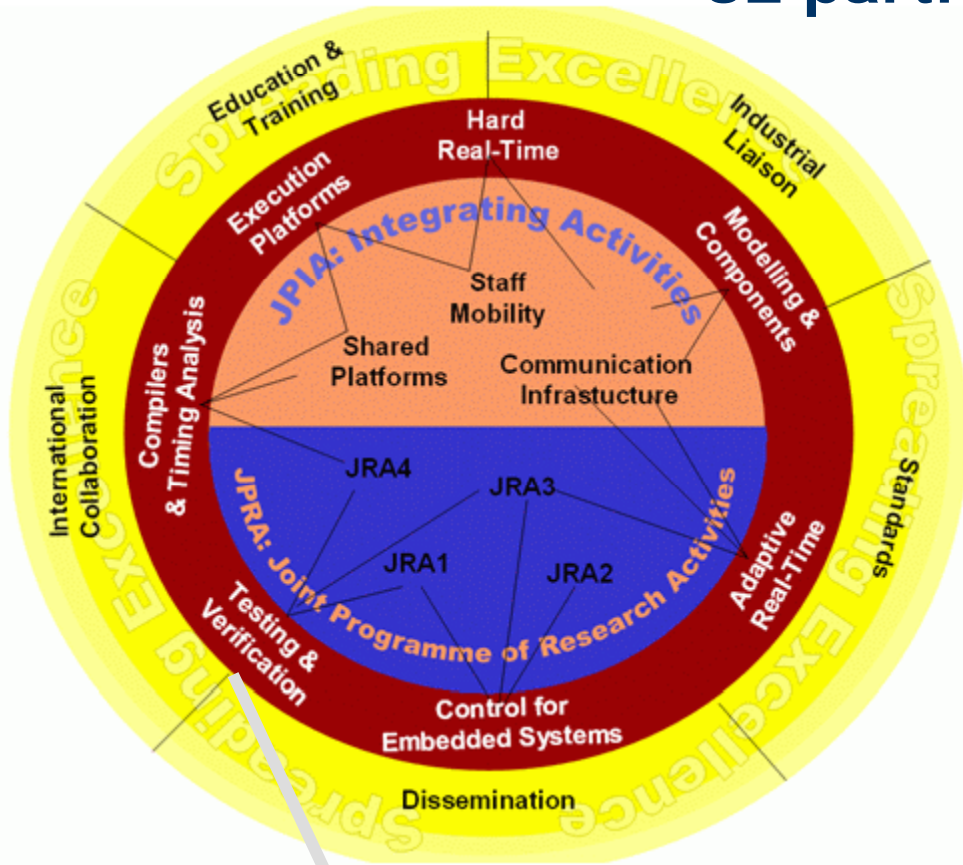
Quasimodo Industrial Handbook

1. Introduction by Brian Nielsen, Jan Tretmans, and Kim Larsen	1
2. Modelling Real-Time Systems using Uppaal by Frits Vaandrager	18
3. More Features in UPPAAL by Alexandre David and Kim G. Larsen	49
4. Industrial Application of Uppaal: The gMAC Synschronization Protocol by Mathijs Schuts, Feng Zhu, Faranak Heidarian and Frits Vaandrager	77
5. Design of a Sage Real-Time Embedded System in Uppaal: The Self-Balancing Scooter Case by Bert Bos, Jiansheng Xing, Teun van Kuppeveld, and Marcel Verhoef	95
6. An Introduction to Schedulability Analysis using Timed Automata by Alexandre David, Arne Skou, and Kim Larsen	107
7. Schedulability Analysis using UPPAAL: The Herschel/Planck Satellite Software Case by Marius Mikucionis, Brian Nielsen, Kim Larsen	119



European Network of Excellence

32 partners



ARTEMIS



Joseph Sifakis

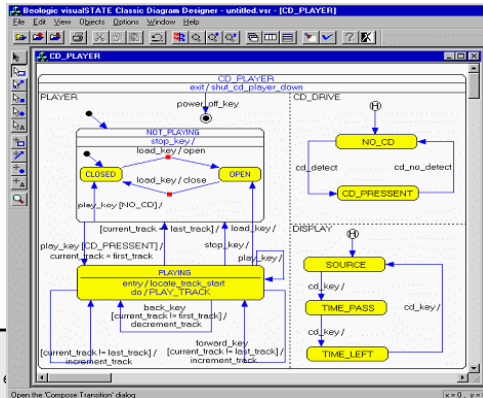
Co-winner of Turing Award 2007

ARTIST Director

**Modeling & Verification
CISS coordinator**

Verification and Testing

Model



```

/* Wait for (
void OS_Wait(void);

/* Operating system visualSTATE process. Mimics a OS process for a
 * visualSTATE system. In this implementation this is the mainloop
 * interfacing to the visualSTATE basic API. */
void OS_VS_Process(void);

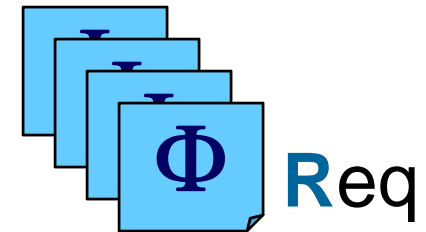
/* Define completion code variable. */
unsigned char cc;

void HandleError(unsigned char ccArg)
{
    printf("Error code %c detected, exiting application.\n", ccArg);
    exit(ccArg);
}

/* In d-241 we only use the OS_Wait call. It is used to simulate a
 * system. Its purpose is to generate events. How this is done is up to
 * you.
 */
void OS_Wait(void)
{
    /* Ignore the parameters; just retrieve events from the keyboard and
     * put them into the queue. When EVENT_UNDEFINED is read from the
     * keyboard, return to the calling process. */
    SEM_EVENT_TYPE event;
    int num;

```

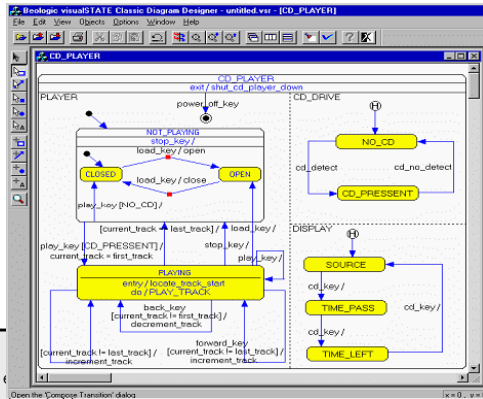
Code



Running System

Verification and Testing

Model



```

/* Wait for (
void OS_Wait(void);

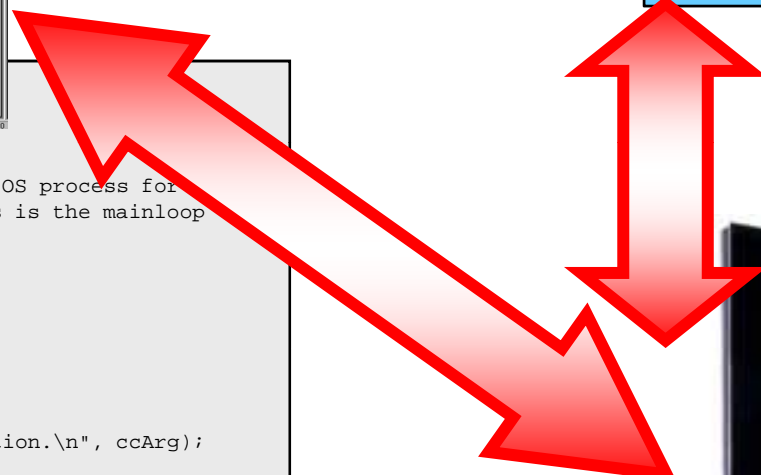
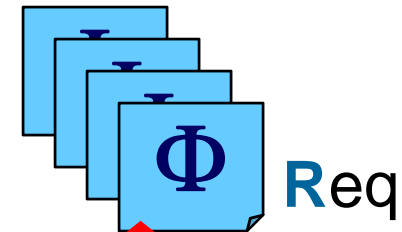
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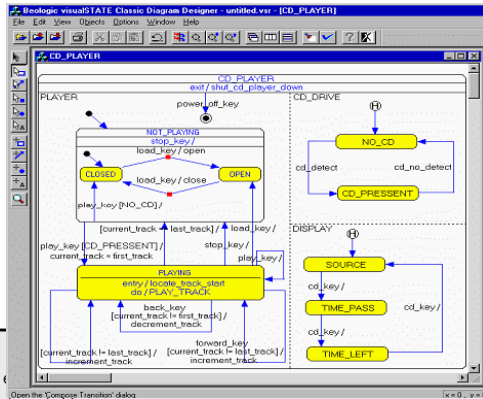
```



Running System

Verification and Testing

Model



```

/* Wait for OS events. */
void OS_Wait(void);

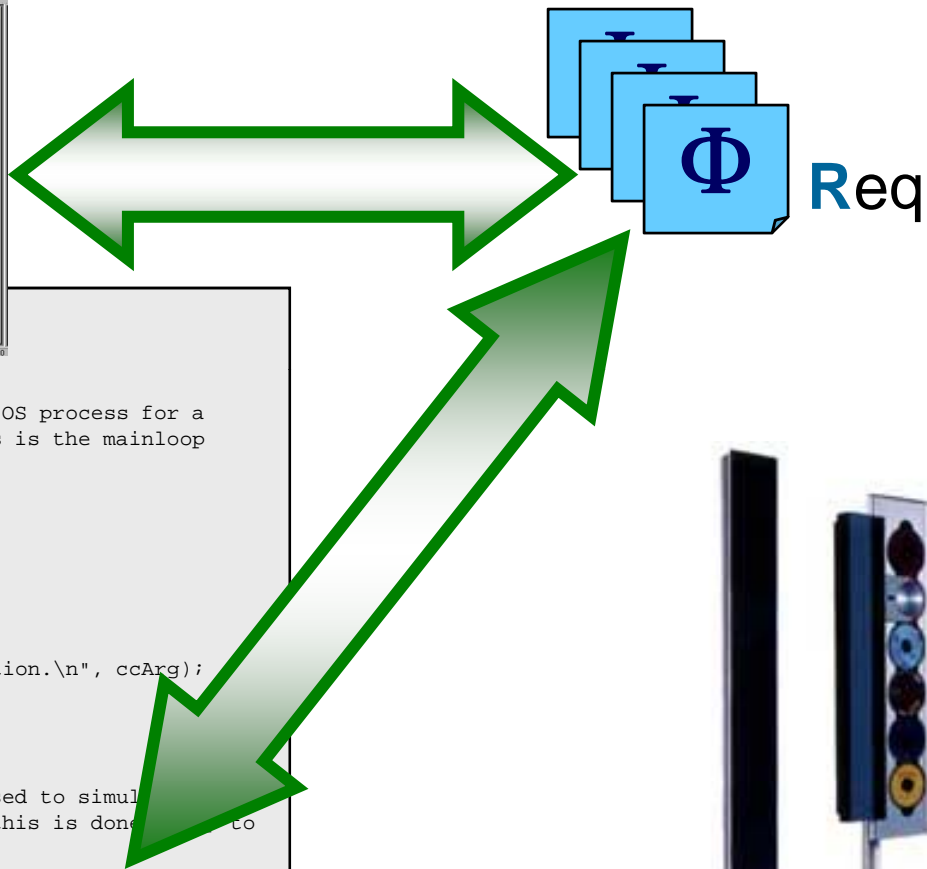
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void HandleError(unsigned char ccArg)
{
    printf("Error code %c detected, exiting application.\n", ccArg);
    exit(ccArg);
}

/* In d-241 we only use the OS_Wait call. It is used to simulate
 * a real OS system. Its purpose is to generate events. How this is done
 * is up to you.
 */
void OS_Wait(void)
{
    /* Ignore the parameters; just retrieve events from the keyboard and
     * put them into the queue. When EVENT_UNDEFINED is read from the
     * keyboard, return to the calling process. */
    SEM_EVENT_TYPE event;
    int num;

```



Running System

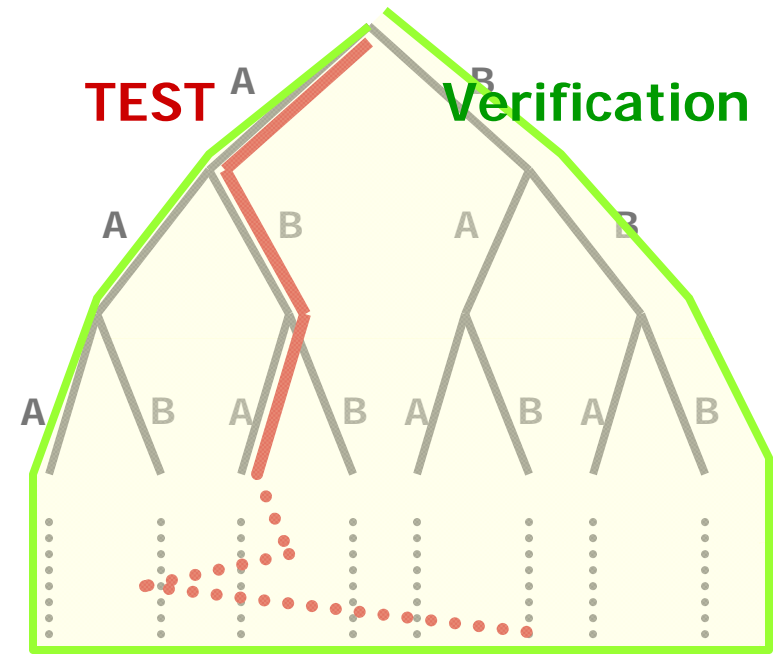
Test versus Verification



E F E E G H ... H A



T1 T3 T5 T1 ... T4 T3



2^n sequences of length n

Deadlock identified using
Verification
 After sequence of
 2000
 telegrams / < 1min



Why Verification and Testing

- 30-40% of production time is currently spend on elaborate, ad-hoc testing:
 - Errors expensive and difficult to fix!
 - The potential of existing/improved testing methods and tools is enormous!
 - Time-to-market may be shortened considerable by verification and performance analyses of early designs!

*** STOP: 0x0000000A (0x802aa502, 0x00000002, 0x00000000, 0xFA84001C)

IRQL_NOT_LESS_OR_EQUAL*** Address fa84001c has base at fa840000 - i8042prt.SYS

CPUID: GenuineIntel 5.2.c irql:1f SYSVER 0xF0000565

Dll Base	Date Stamp	- Name	Dll Base	Date Stamp	- Name
80100000	2be154c9	- ntoskrnl.exe	80400000	2bc153b0	- hal.dll
80200000	2bd49628	- ncr710.sys	8025c000	2bd49688	- SCSIPTORT.SYS
80267000	2bd49683	- scsidisk.sys	802a6000	2bd496b9	- Fastfat.sys
fa800000	2bd49666	- Floppy.SYS	fa810000	2bd496db	- Hpfs_Rec.SYS
fa820000	2bd49676	- Null.SYS	fa830000	2bd4965a	- Beep.SYS
fa840000	2bdaab00	- i8042prt.SYS	fa850000	2bd5a020	- SERMOUSE.SYS
fa860000	2bd4966f	- kbdclass.SYS	fa870000	2bd49671	- MOUCLASS.SYS
fa880000	2bd9c0be	- Videoprt.SYS	fa890000	2bd49638	- NCR77C22.SYS
fa8a0000	2bd4a4ce	- Vga.SYS	fa8b0000	2bd496d0	- Msfs.SYS
fa8c0000	2bd496c3	- Npfs.SYS	fa8e0000	2bd496c9	- Ntfs.SYS
fa940000	2bd496df	- NDIS.SYS	fa930000	2bd49707	- wlan.sys
fa970000	2bd49712	- TDI.SYS	fa950000	2bd5a7fb	- nbfs.sys
fa980000	2bd72406	- streamio.sys	fa9b0000	2bd4975f	- ubnh.sys
fa9c0000	2bd5bfd7	- mcsxms.sys	fa9d0000	2bd4971d	- netbios.sys
fa9e0000	2bd49678	- Parallel.sys	fa9f0000	2bd4969f	- serial.SYS
faa00000	2bd49739	- mup.sys	faa40000	2bd4971f	- SMBTRSUP.SYS
faa10000	2bd6f2a2	- srv.sys	faa50000	2bd4971a	- afd.sys
faa60000	2bd6fd80	- rdr.sys	faaa0000	2bd49735	- browser.sys

Address	dword	dump	Build [1381]	- Name
fe9cdaec	fa84003c	fa84003c	00000000 00000000	80149905 - i8042prt.SYS
fe9cdfaf8	8025dfe0	8025dfe0	ff8e6b8c 80129c2c	ff8e6b94 - SCSIPTORT.SYS
fe9cdb10	8013e53a	8013e53a	ff8e6b94 00000000	ff8e6b94 - ntoskrnl.exe
fe9cdb18	8010a373	8010a373	ff8e6df4 ff8e6f60	ff8e6c58 - ntoskrnl.exe
fe9cdb38	80105683	80105683	ff8e6f60 ff8e6c3c	8015ac7e - ntoskrnl.exe
fe9cdb44	80104722	80104722	ff8e6df4 ff8e6f60	ff8e6c58 - ntoskrnl.exe
fe9cdb4c	8012034c	8012034c	00000000 80088000	80106fc0 - ntoskrnl.exe

Why Verification and Testing

■ IMPORTANCE for EMBEDDED SYSTEMS

- Often safety critical
- Often economical critical
- Hard to patch



■ CHALLENGES for EMBEDDED SYSTEMS

- Correctness of embedded systems depend crucially on use of *resources*
e.g. real-time, memory, bandwidth, energy.
- Need for *quantitative models*

Spectacular software bugs

Ariane 5

- The first Ariane 5 rocket was launched in June, 1996. It used software developed for the successful Ariane 4. The rocket carried two computers, providing a backup in case one computer failed during launch. Forty seconds into its maiden flight, the rocket veered off course and exploded. The rocket, along with \$500 million worth of satellites, was destroyed.



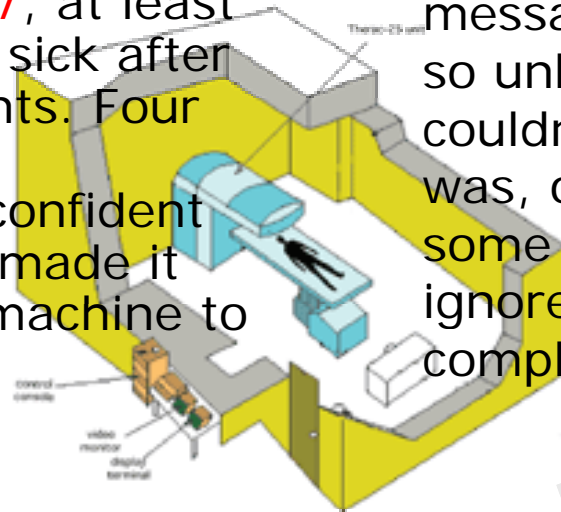
- Ariane 5 was a much more powerful rocket and generated forces that were larger than the computer could handle. Shortly after launch, it received an input value that was too large. The main and backup computers shut down, causing the rocket to veer off course.

Spectacular software bugs

Therac 25

Safety Critical

- The Therac-25 radiation therapy machine was a medical device that used beams of electrons or photons to kill cancer cells. Between 1985-1987, at least six people got very sick after Therac-25 treatments. Four of them died. The manufacturer was confident that their software made it impossible for the machine to harm patients.



- The Therac-25 was withdrawn from use after it was determined that it could deliver fatal overdoses under certain conditions. The software would shut down the machine before delivering an overdose, but the error messages it displayed were so unhelpful that operators couldn't tell what the error was, or how serious it was. In some cases, operators ignored the message completely.

"H-tilt"

"Malfunction 54"

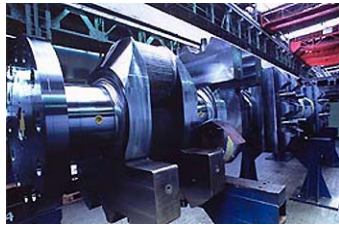
IEEE Computer, Vol. 26, No. 7, July 1993, pp. 18-41

Spectacular Software Bugs

.... continued

- INTEL Pentium II floating-point division
470 Mill US \$
- Baggage handling system, Denver
1.1 Mill US \$/day for 9 months
- Mars Pathfinder
-

ES are Pervasive



• Characteristica:

- Dedicated function
- Complex environment
- SW/HW/Mechanics
- Autonomous
- Ressource constrained
 - : Energy
 - : Bandwidth
 - : Memory
 - : ...
- **Timing constraints**

ES are often Safety Critical



- 300 horse power
- 100 processors

- How to achieve ES that are:

- correct
- predicabile
- dependable
- fault tolerant
- ressource minial
- cheap

- Model-Based Development



A simple program

```
int x=100;

Process INC
  do
  :: x<200 --> x:=x+1
  od

Process DEC
  do
  :: x>0 --> x:=x-1
  od

Process RESET
  do
  :: x=200 --> x:=0
  od

( INC || DEC || RESET )
```

Which values may
x take ?

Questions/Properties:

E<>(x>100)

E<>(x>200)

A[](x<=200)

E<>(x<0)

A[](x>=0)

Possibly

Always

Another simple program

What are the possible final values of x ?

```
int x=0;

Process P
do
    x:=x+1
10 times

( P || P )
```

```
int x=0;

Process P
int r
do
    r:=x; r++; x:=r
10 times

( P || P )
```

Atomic stm

Yet another simple program

```
int x=1;

Process P
do
    x:=x+x
forever

( P || P )
```

What are the possible values that x may posses during execution?

```
int x=1;

Process P
int r
do
    r:=x; r:=x+r; x:=r
forever

( P || P )
```

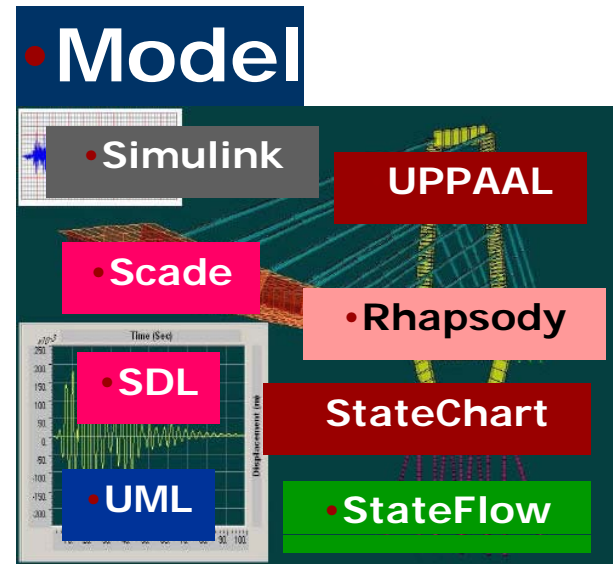
Atomic stm

Model-based Approach

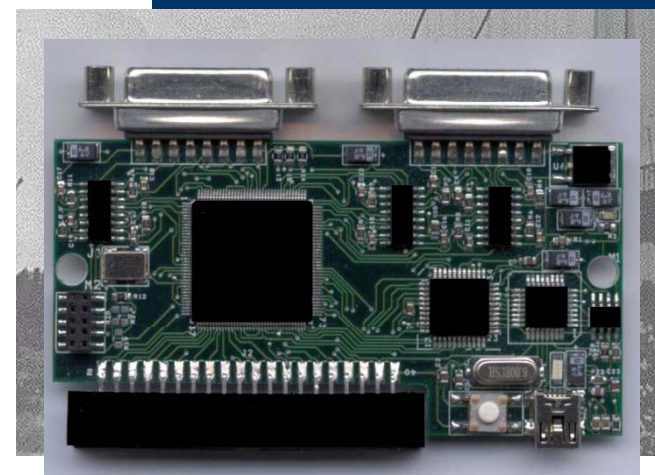


Models

- A model is a simplified representation of the real world.
- User gains confidence in the adequacy and validity of a proposed system.
- Models selected aspects. Removes irrelevant details.
- Early design exploration.

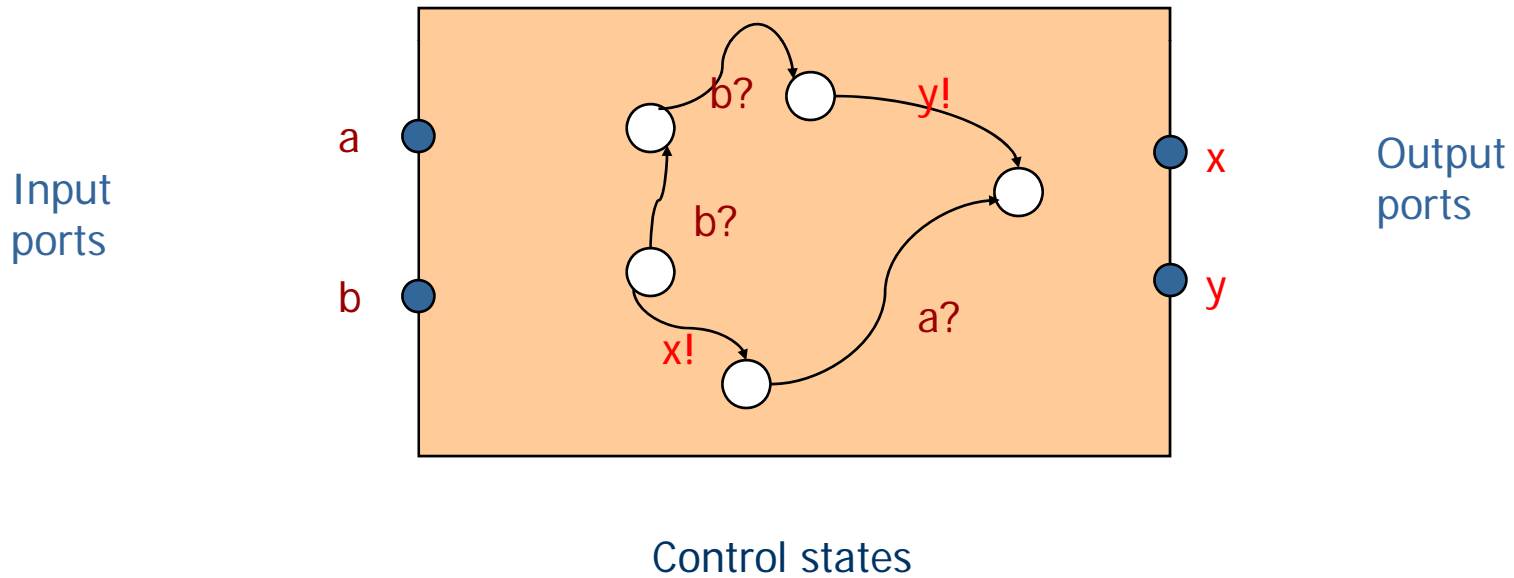


Realization

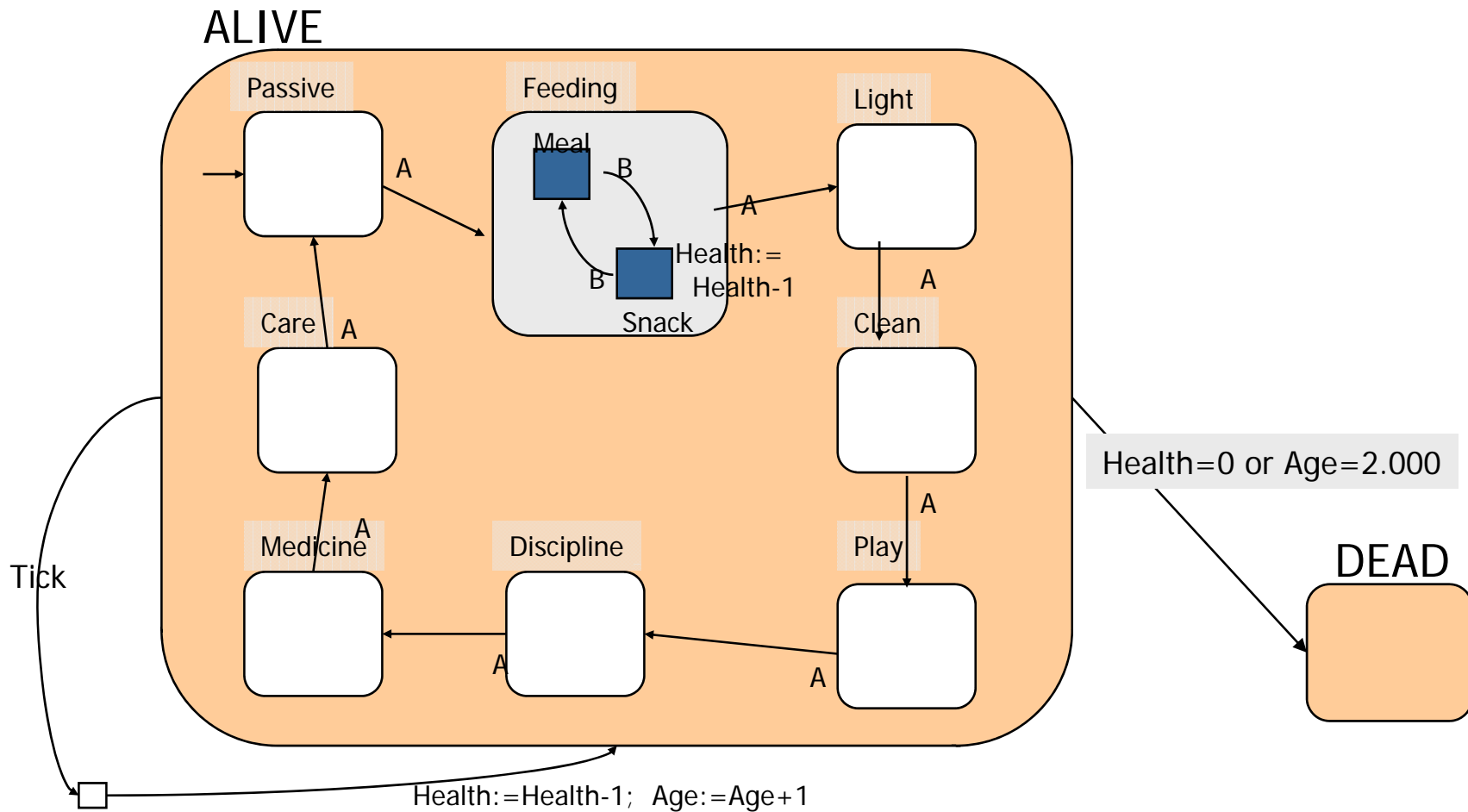
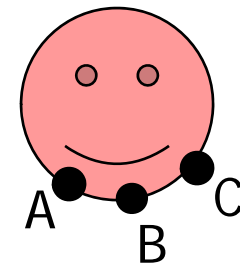


How?

Unified Model = State Machine!



Tamagotchi



Digital Watch – UML Statechart

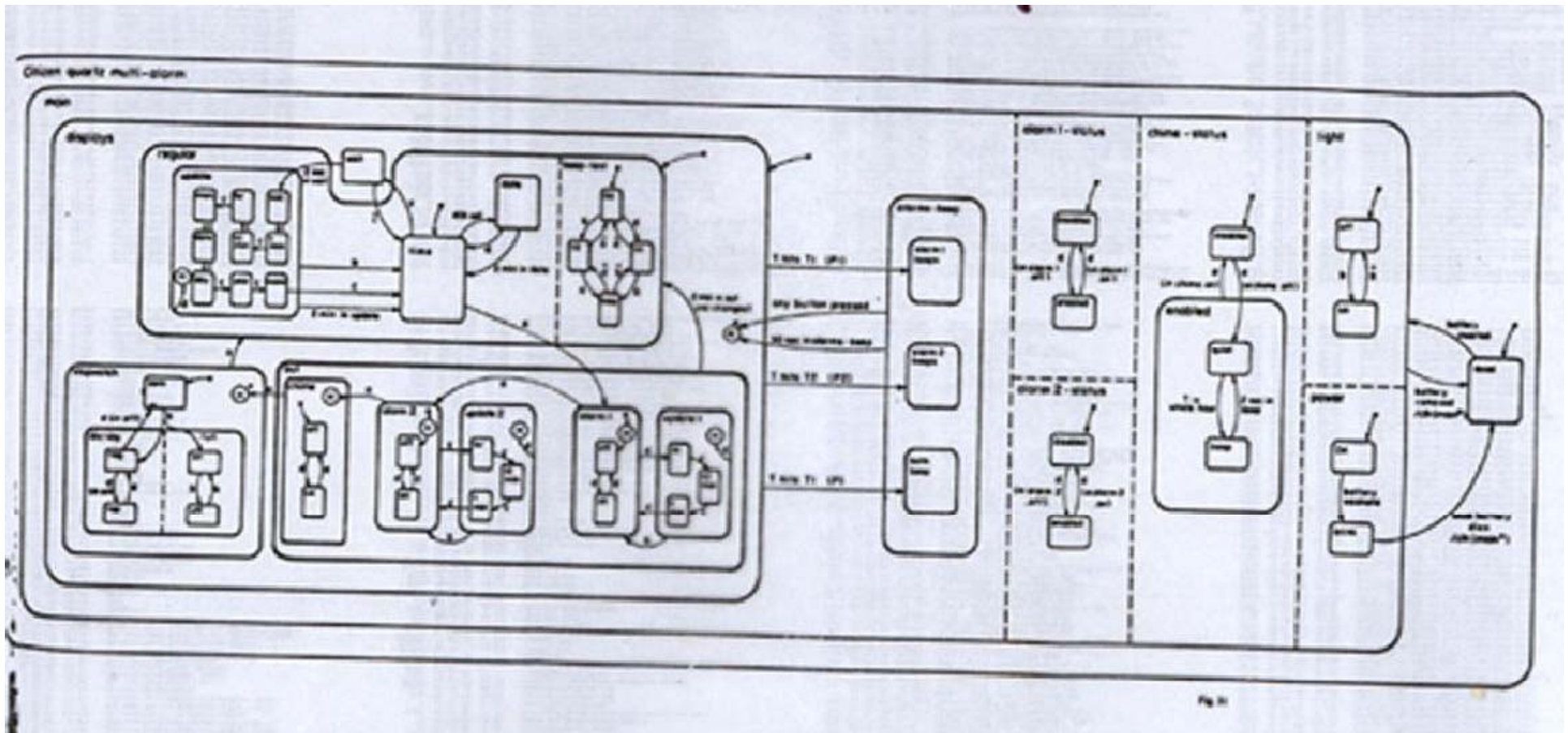


Fig. 20

```

SPIN CONTROL 3.1.3 -- 16 March 1998 -- File: p123
File.. Edit.. Run.. Help  SPIN DESIGN VERIFICATION  Line#: 18  Find:
mtype = { msg0, msg1, ack0, ack1 };
chan  sender =[1] of { byte };
chan  receiver=[1] of { byte };

proctype Sender()
{
  byte any;
again:
  do
    :: receiver!msg1;
    if
      :: sender?ack1 -> break
      :: sender?any /* lost */
      :: timeout /* retransmit */
    fi
  od;
  do
    :: receiver!msg0;
    if
      :: sender?ack0 -> break
      :: sender?any /* lost */
      :: timeout /* retransmit */
    fi
  od;
  goto again
}

proctype Receiver()
{
  byte any;
again:
  do
    :: receiver?msg1 -> sender!ack1; break
    :: receiver?msg0 -> sender!ack0
    :: receiver?any /* lost */
  od;
P0:
  do
    :: receiver?msg0 -> sender!ack0; break
  od;
}

```

<starting simulation>
 /pack/PS/Spin.prog/spin-3.13/bin/spin -X -p -v -g -l -s -r -t -j0 pan_in
 <at end of trail>

```

) line 41 "pan_in" (state 16)
line 23 "pan_in" (state 16)
line 50 "pan_in" (state 4)

ne 63 "never" (state 0) [printf('MSC:
line 63 "pan_in" (sta

```

Message Sequence Chart details:
 - Lifelines: Sender, Receiver, receiver!msg1
 - Messages: 1 (init:1), 3, 4, 5, 7, 9, 11, 13, 14, 15, 17, 21, 22, 23, 24, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 51, 53, 55, 57, 59, 63, 65
 - Cycle: Indicated at the end of the sequence.

```

Verification Output
warning: for p.o. reduction to be valid the never claim must be stutter-closed
(never claims generated from LTL formulae are stutter-closed)
pan: acceptance cycle (at depth 59)
pan: wrote pan_in.trail
(Spin Version 3.1.3 -- 16 March 1998)
Warning: Search not completed
+ Partial Order Reduction

Full statespace search for:
  never-claim          +
  assertion violations + (if within scope of claim)
  acceptance cycles   + (fairness disabled)
  invalid endstates   - (disabled by never-claim)

State-vector 32 byte, depth reached 67, errors: 1
  35 states, stored (41 visited)
   6 states, matched
  47 transitions (= visited+matched)
   1 atomic steps
hash conflicts: 0 (resolved)
(max size 2^19 states)

2.542 memory usage (Mbyte)

```

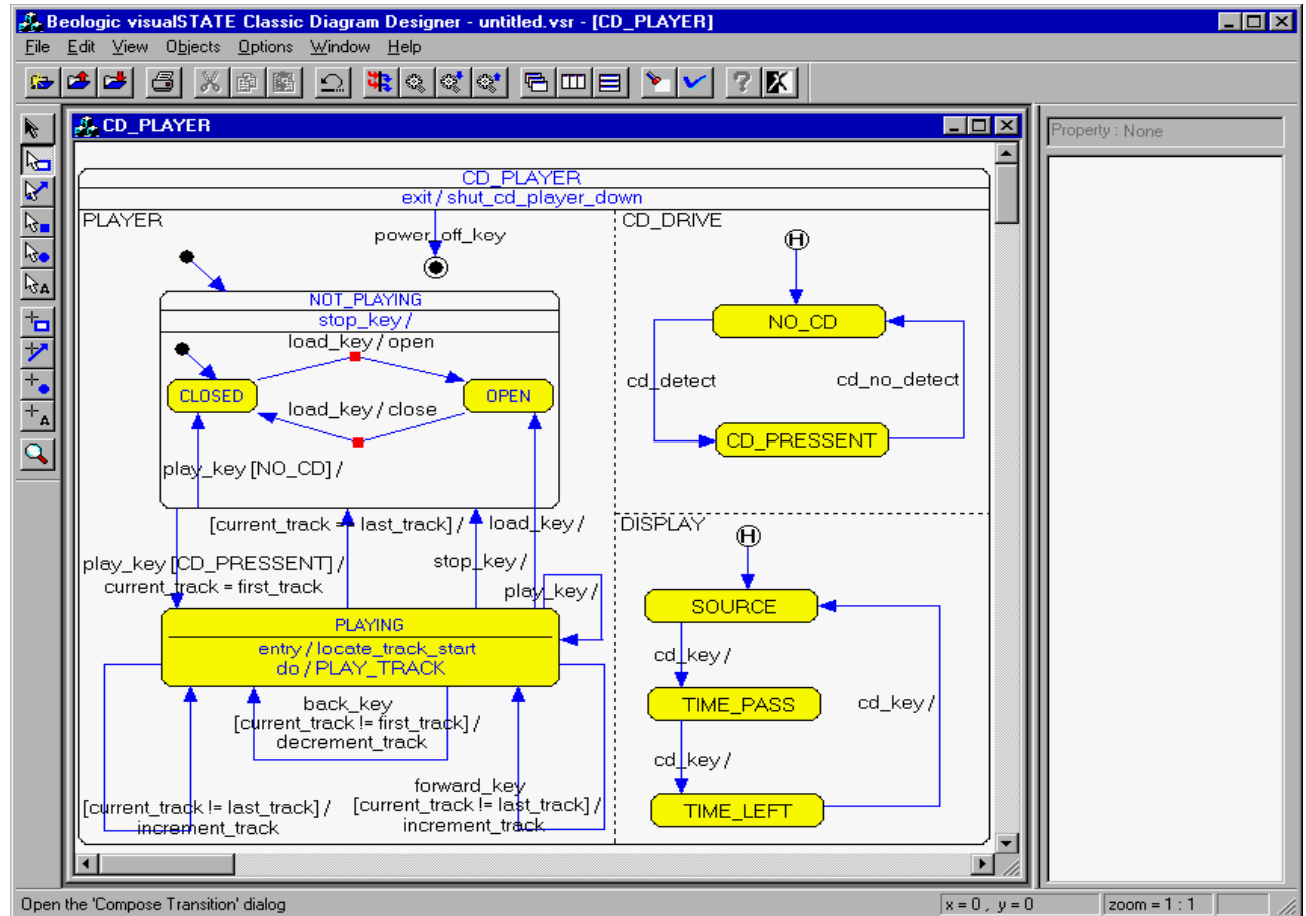
visualSTATE

VVS

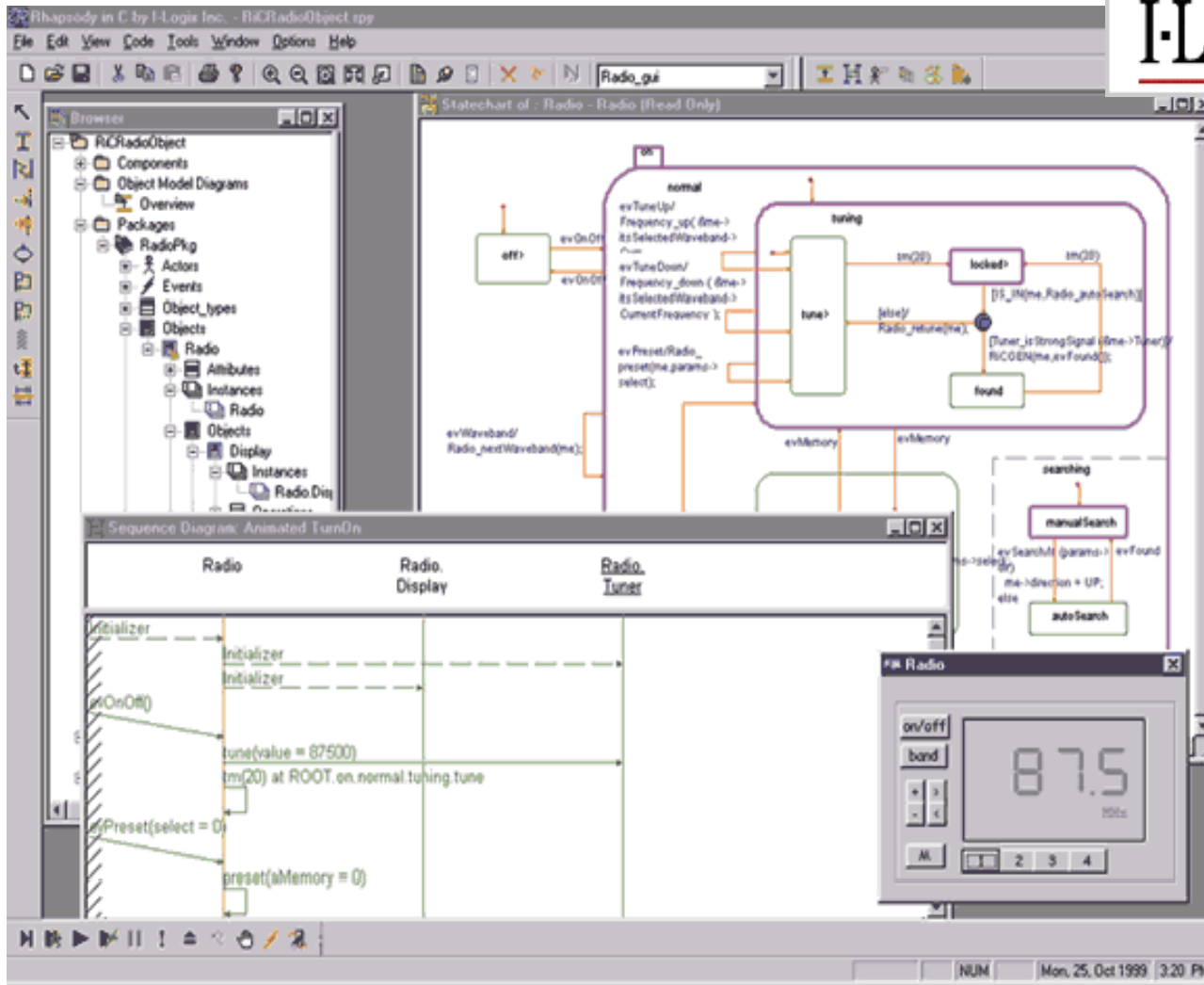
w Baan Visualstate, DTU (CIT project)



- Hierarchical state systems
- Flat state systems
- Multiple and inter-related state machines
- Supports UML notation
- Device driver access



Rhapsody



ESTEREL

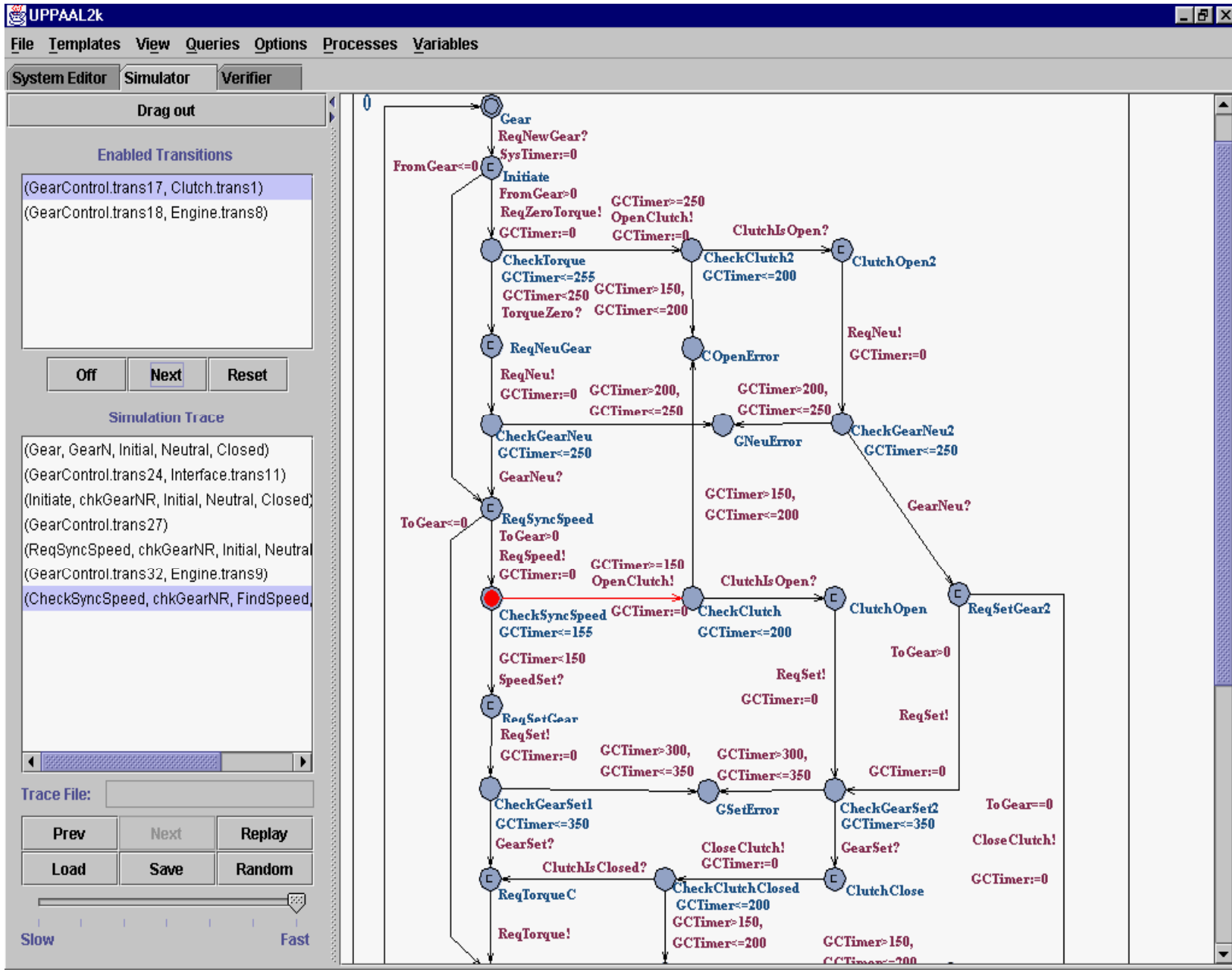
The image displays the ESTEREL IDE interface with several windows open:

- Simulation Output:** A table showing the current state of the simulation.

Name	Value	Type
RingBell		
TILT		
GameOver		
Go		
Display	.*	integer
GameNormal.RemainingMe	.*	integer
- Simulation Control:** A control panel for the simulation.

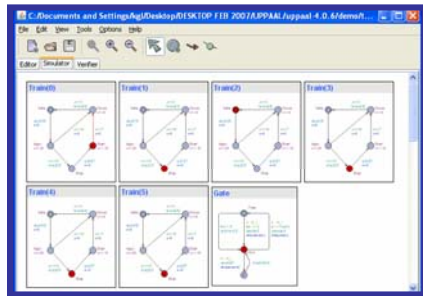
Name	Value	Type
Coin		
On_off		
Ready		
Stop		
MS		
- ReflexGameNormal (Main Diagram):** A state transition diagram for the ReflexGameNormal module. It shows a state with an initial state (I) and a transition labeled "On_off/".
- MachineON:** A sub-diagram showing a state with an initial state (I) and a transition labeled "On_off/". It includes a "Game Over" state with the text "sustain GameOver".
- GAME:** A sub-diagram showing a state with a coin (C) and a transition labeled "Coin/". It includes a "PAUSE_LENGTH MS/ Display(?MEAN/MEASURE_NUMBER)" state.

The main diagram also shows a signal definition: `signal RemainingMeasures:integer, MEAN:integer` and a transition labeled `/Display(0), 'call InitRNDGenerator()'`.



UPPAAL

QUANTITATIVE Model Checking



System Description



Time



Cost



Probability



No!

Debugging Information

Yes

Prototypes
Executable Code
Test sequences

Requirement

$A \square (\text{req} \Rightarrow A \diamond \text{grant})$

$A \square (\text{req} \Rightarrow A \diamond_{t < 30s} \text{grant})$

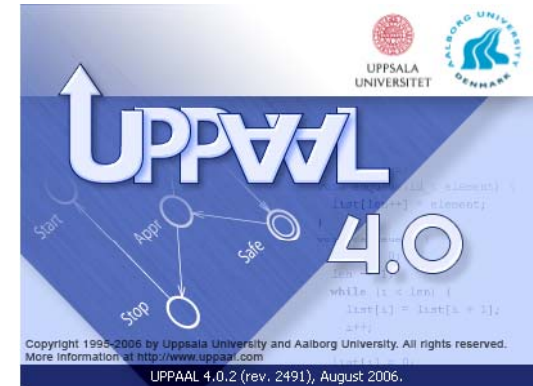
$A \square (\text{req} \Rightarrow A \diamond_{t < 30s, c < 5\$} \text{grant})$

$A \square (\text{req} \Rightarrow A \diamond_{t < 30s, p > 0.90} \text{grant})$

UPPAAL Branches

CLASSIC

- Real Time Modelling & Verification
Decidability Engine



- Real Time Scheduling & Schedulability Analysis

CORA

- Real Time Controller Synthesis
Compositionality

TIGA

ECDAR

- Real Time Testing
Performance Analysis

TRON

SMC

Slides, Reading Material, Exer ...

www.cs.aau.dk/~kgl/China11



The screenshot shows a web browser window with the following content:

- Address bar: <http://www.cs.aau.dk/~kgl/China2011/>
- Navigation buttons: Back, Forward, Refresh, Home, Stop
- Open tabs: 404 Not Found, Exercises, Reading material, Reading material
- Slide title: **Validation, Synthesis** and **Performance Evaluation** of **Embedded Systems** using UPPAAL
- Authors: Three cartoon avatars, a real photo of Kim Guldstrand Larsen, and two more cartoon avatars.
- Author name: **Kim Guldstrand Larsen**
- Affiliation: CISS, Aalborg University, DENMARK
- Date: Beijing, August 8-12, 2011.

[.../Material.html](#)
[../Exercises.html](#)